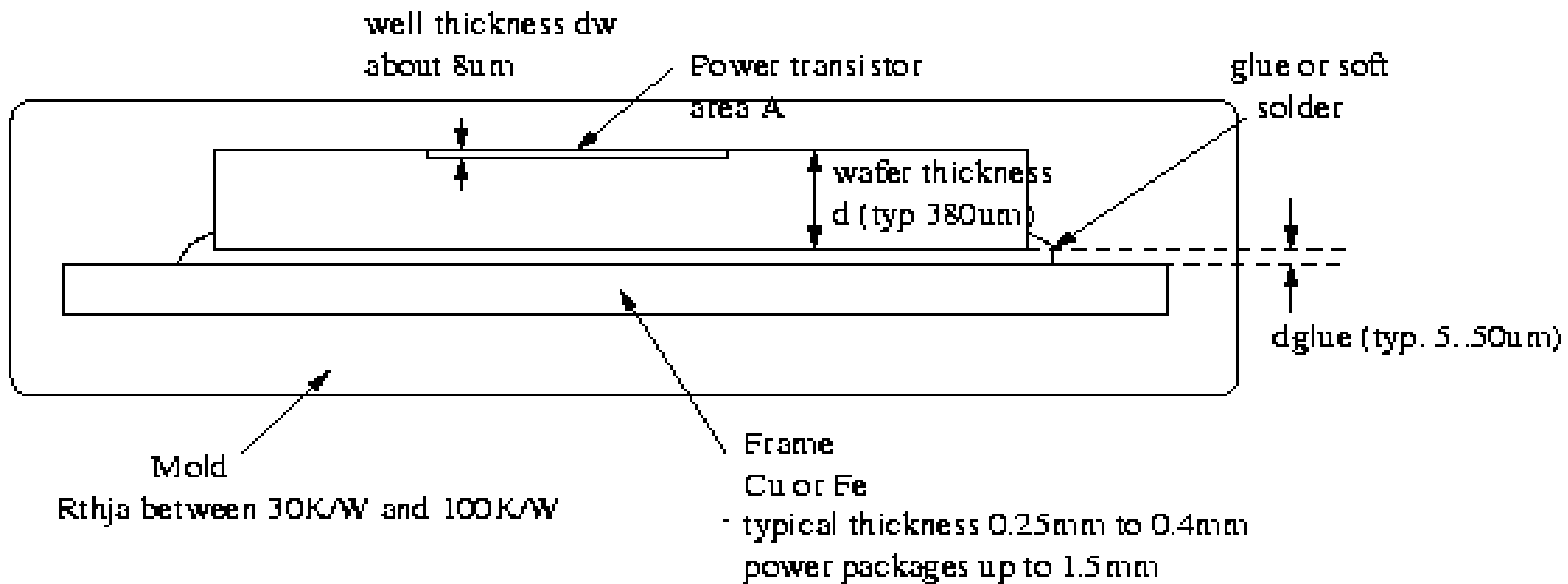
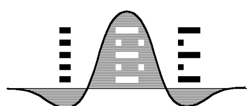
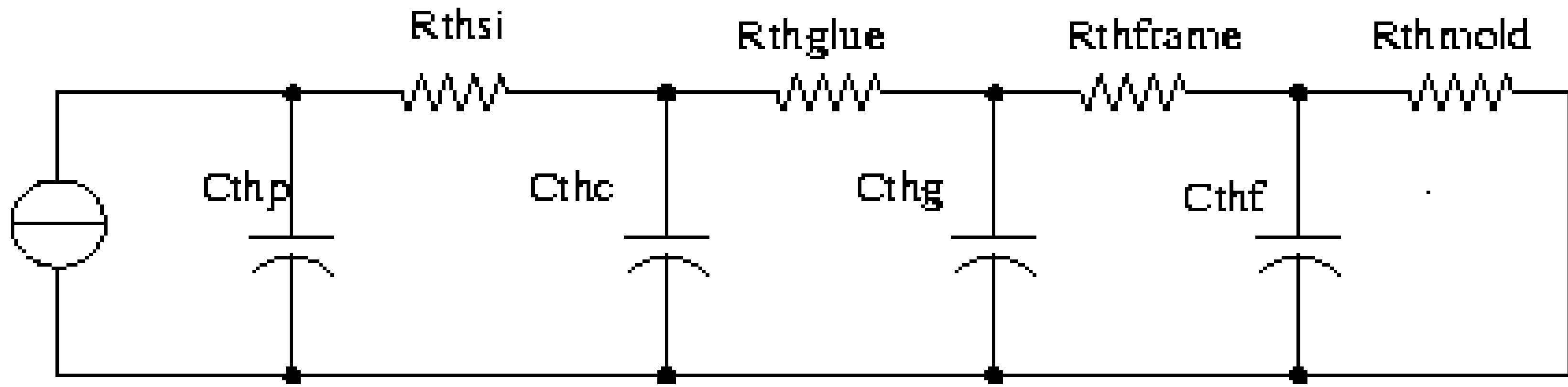
Power Chip Inside the Package





One Dimensional Approximation for Large Transistors



$Cthp = A * dw * \rho_{Si} * c$

$Rthsi = d/(A * \lambda_{Si})$

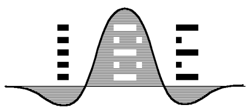
$Cthc = A * d * \rho * c_{Si}$

$Rthglue = dglue/(A * \lambda)$

$Rthframe = df/(A * \lambda_{Fe})$

$Cthf = A * df * \rho_{Fe} * c$

Silicon: 100°C	Iron: 100°C
$\rho_{Si} = 2.3 * 10^3$ kg m^{-3}	$\rho_{Fe} = 7.4 * 10^3$ kg m^{-3}
$c_{Si} = 760$ Ws kg^{-1} K^{-1}	$c_{Fe} = 452$Ws kg^{-1} K^{-1}
$\lambda_{Si} = 110$W $m^{-1} K^{-1}$	$\lambda_{Fe} = 74$W $m^{-1} K^{-1}$



Ingenieurbüro Erckert
Ricardo Erckert

Example: $10mm^2$ Power Transistor

$Cthp=A*dw*\rho_{Si}*c = 1.3984^{-4}$ Ws/K

$Rthsi=d/(A*\lambda_{Si}) = 0.3454$ K/W

$Cthc=A*d*\rho*c_{Si} = 6.642^{-3}$ Ws/K

$Rthglue=dglue/(A*\lambda) = 2$K/W

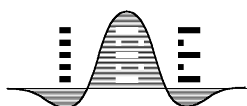
$Rthframe=df/(A*\lambda_{Fe}) = 0.3378$ K/W (0.25mm Fe)

$Cthf= A*df*\rho_{Fe}*c = 8.362^{-3}$ Ws/K

$Rthca = 30$K/W

–> Rthja=32.68K/W but Rthjc=2.68K/W

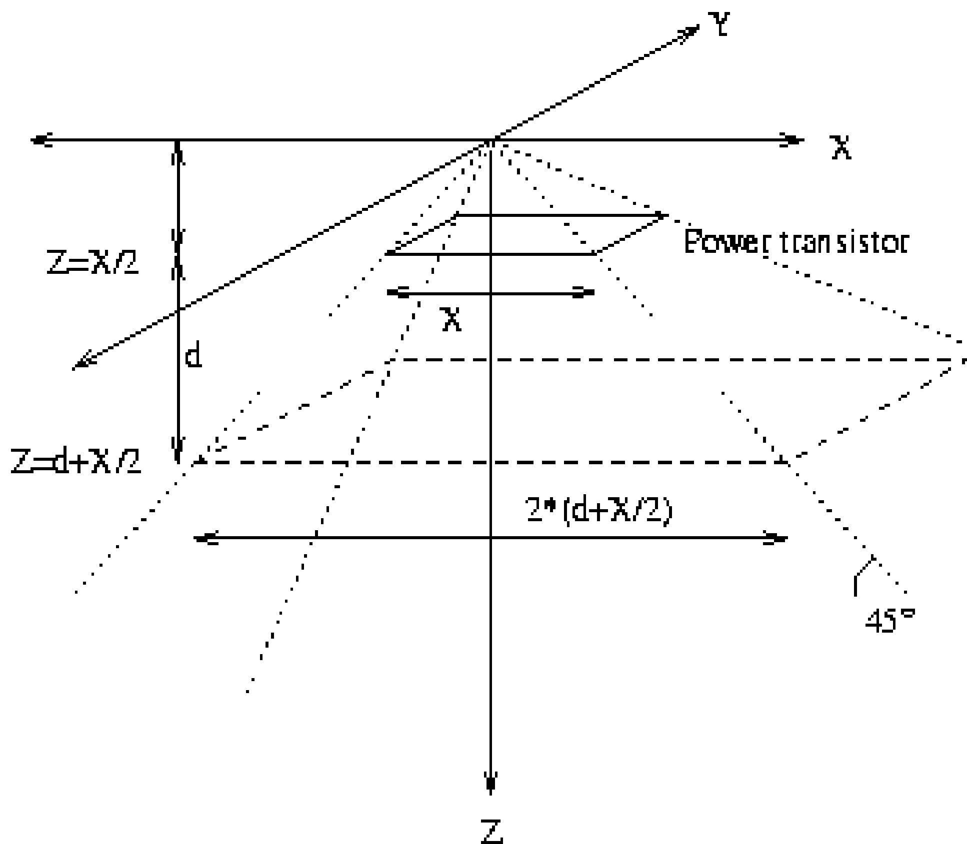
(Assumption: λglue=0.5Ws $m^{-1}K^{-1}$, dglue=10μm)



Ingenieurbüro Erckert
Ricardo Erckert

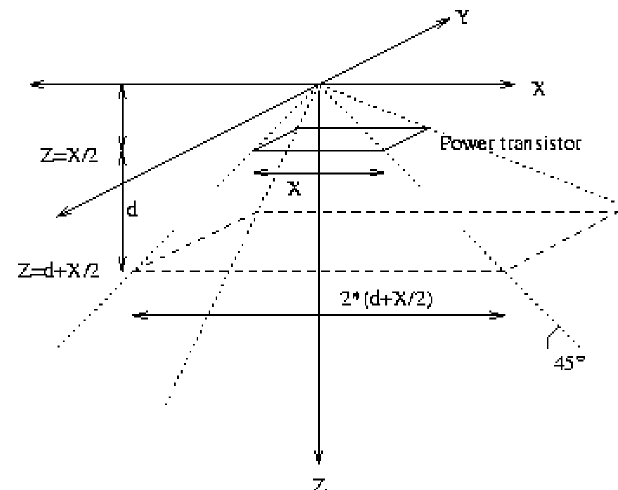
Small Power Transistors

If the power transistor is small (side shorter than 3 times the wafer thickness) a more refined approximation is needed. The heat follows through a pyramid and the flow density decreases with increasing distance.



Small Power Transistors

For square shaped transistors the heat flows through a pyramid that can be aproximated as:



$A(z) = (2^*z)^2$

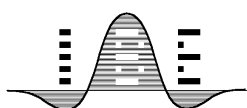
The differential thermal resistance becomes:

$dR_{th}=dz/(4z^2*\lambda)$

Integrating Rth from z=X/2 to z=d+X/2 leads to the thermal resisatance from the silicon surface to the backside of the chip.

$$Rth = \frac{1}{(4*\lambda)} * \int \left(\frac{dz}{z^2}\right)$$

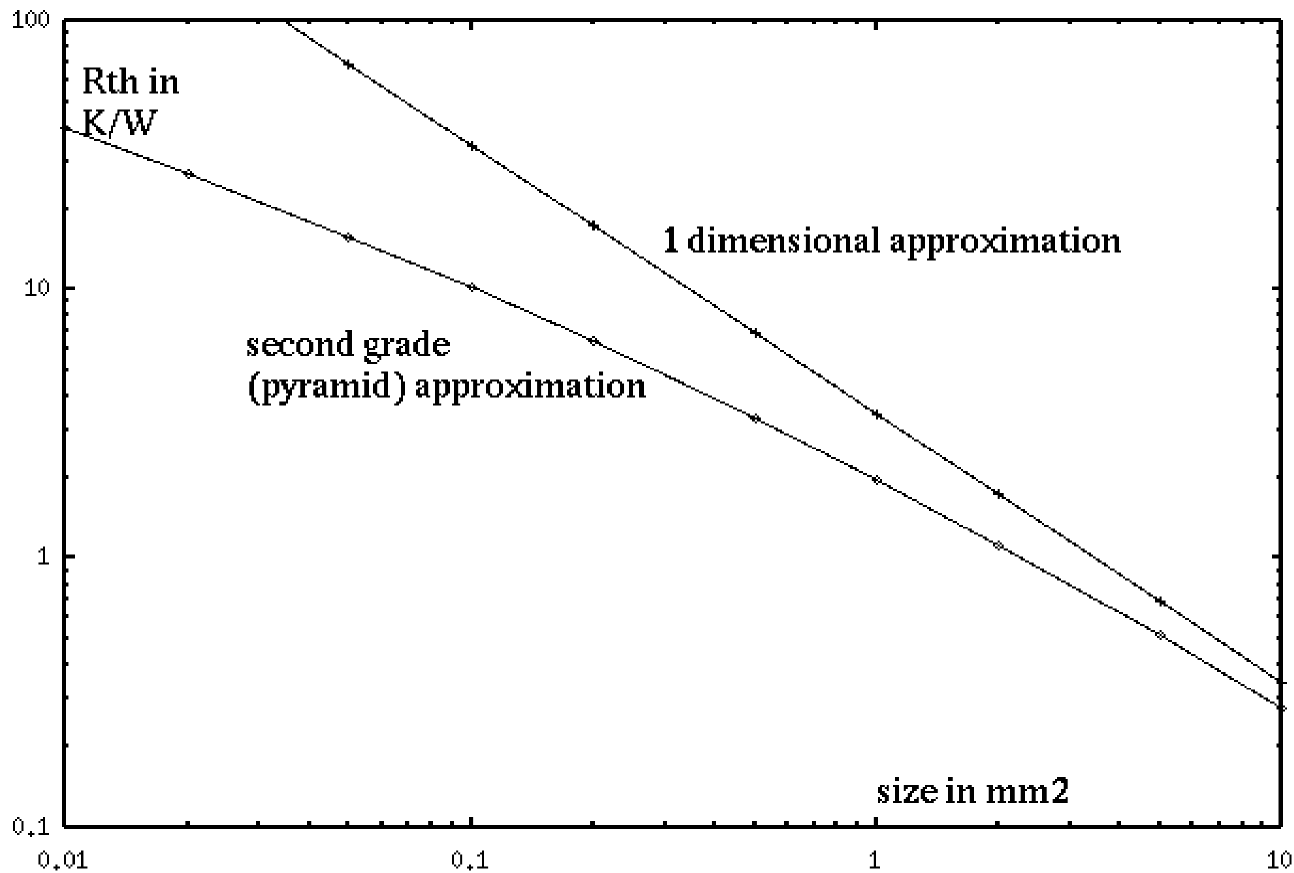
$Rth=[2/x+1/(d+0.5*x)] / (4*\lambda)$

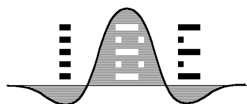


Ingenieurbüro Erckert
Ricardo Erckert

Small Power Transistors

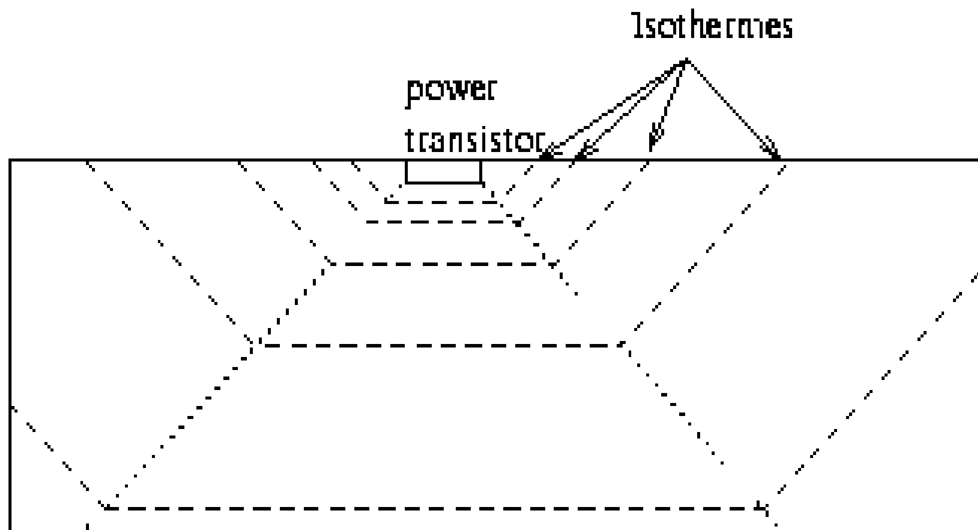
Rth through a 380 µm wafer w.r.t. power transistor size





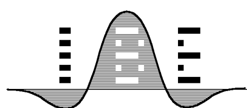
Temperature Distributions

first grade approximation of Isothermes

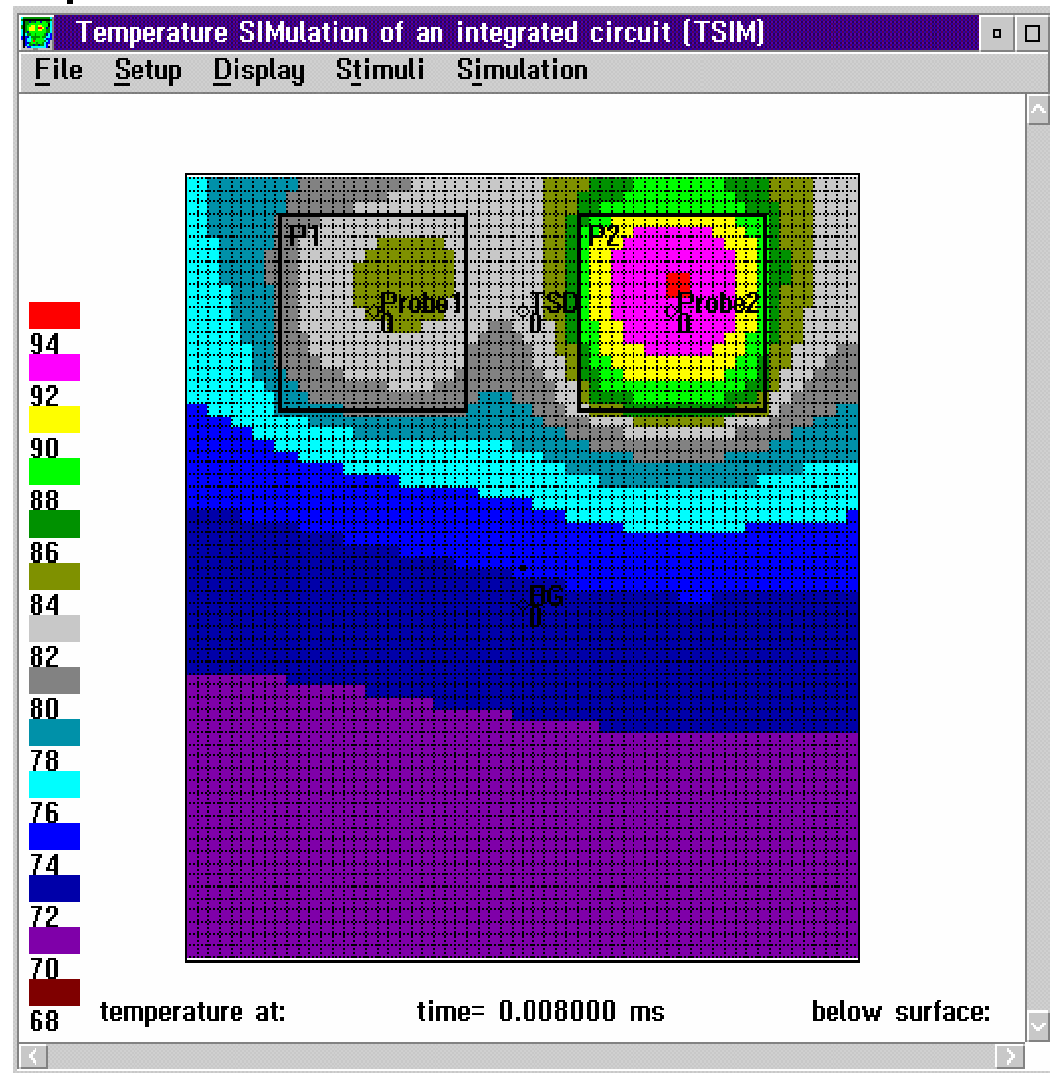


areas further away from the power transistor than double the wafer thickness thermally follow the frame.

More accurat calculation requires finite element approaches.



Temperature Distributions



Simulation of a chip, 4mm^2,
P1: 0.25mm^2, 1W,
P2: 0.25mm^2, 2W

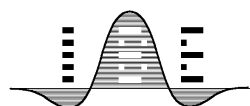
grit: 30µm

frame: 1.5mm copper
(power SO package)

frame temperature 60°C

wafer thickness 380µm

attachment: glue



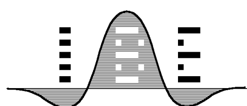
Ingenieurbüro Erckert
Ricardo Erckert

05.03.02

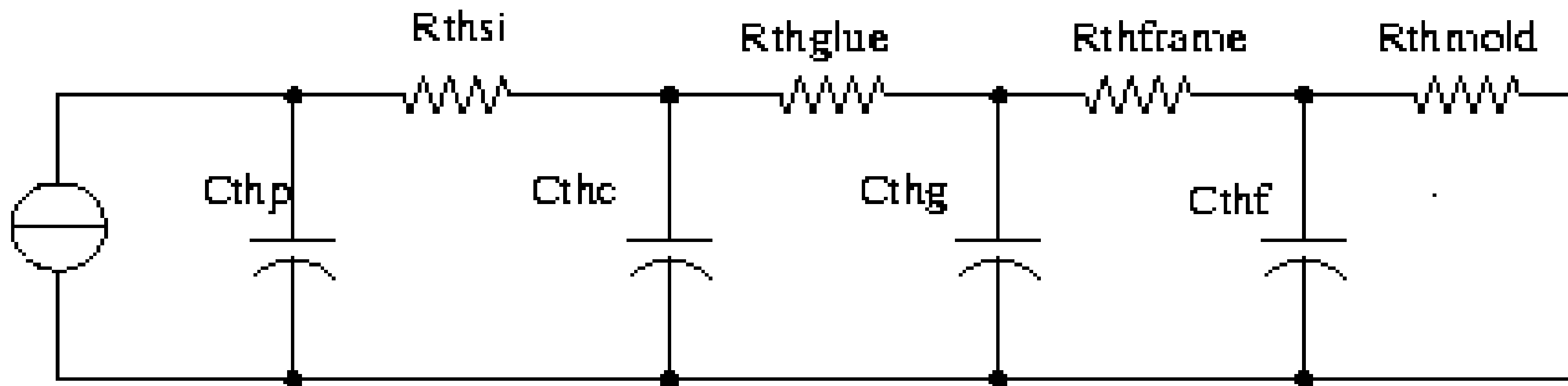
Impact of Temperature Distributions on IC Performance

On silicon

- Leakage doubles all 6K
  (typical 0.7µm MOS 1nA , bipolar about 30nA at 150°C)
- Current capability of AlSi wires half all 6K
- Resistors change between 0 and 0.7% per K
- Rdson increases by 0.3%/K
- Vbe changess typically by –2mV/K
- MOS thresholds change between –2mV/K and –5mV/K
- gain of amplifiers (gm) decreases about –0.3%/K
- Usual package mold granulates at about 180°C
- AlSi alloy melts at about 450°C
- Pure silicon melts at about 1420°C



Typical Time Constants (Example: $10mm^2$ Transistor)



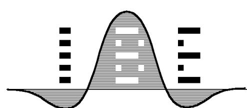
T1=Cthp*Rthsi=0.06ms (Takes short pulses)

T2=Cthc*Rthsi*Rthglue/(Rthsi+Rthglue)=2.03ms

T3=Cthf*Rthmold=0.1s to 5s depending on the package

ESD pulse are absorbed by the silicon volume at the junction!

Example: $0.01mm^2$ junction area, 5µm deep –> Cthp=0.08µWs/K
a 2kV HMB (2A), 40V clamping is 16µWs –> ΔT=200K



Transient Thermal Simulation

LinePlot - [untitled]

File Parameters Options Help

Transient thermal response

P1 switching from 1W to 10W at t=0.01ms

P2 switching from 1W to 10W at t=5ms

TSD

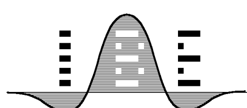
Bandgap

Temperature in °C

260 240 220 200 180 160 140 120 100 80 60

0 1 2 3 4 5 6 7 8 9 10

Time in ms



Ingenieurbüro Erckert

Ricardo Erckert

Typical Power Densities

Component	***Power density***	***Thermal protection***
Lateral PNP (DOPL)	$20W/mm^2$	May be anywhere on the chip
Vertical PNP (HDS2P2)	$40W/mm^2$	Current limit and temperature sensor closer than 150µm
NPN (DOPL)	$30W/mm^2$	DC operating, Emitter resistors, sensor closer than 40µm
NPN (DOPL)	$500W/mm^2$	Turn off immediatelly ($t_{delay}<3\mu s$) after short and don't allow duty cycle higher than 10%. Thermal sensor is too slow.
DMOS (BCD2)	$250W/mm^2$	Closer than 40µm
LDMOS (BCD3)	$900W/mm^2$	Inside power transistor or turn off immediatelly ($t_{delay}<3\mu s$) after short and don't allow duty cycle higher than 10%