Generic Technology Cross Sections and Associated Parasitic Components

This Document describes the components present in most high voltage technologies including the associated parasitic components. Generally it is assumed that a P-substrate is used.

Contents

Overview

The following figure gives an overview of typical low voltage CMOS and high voltage CMOS components available in most technologies.

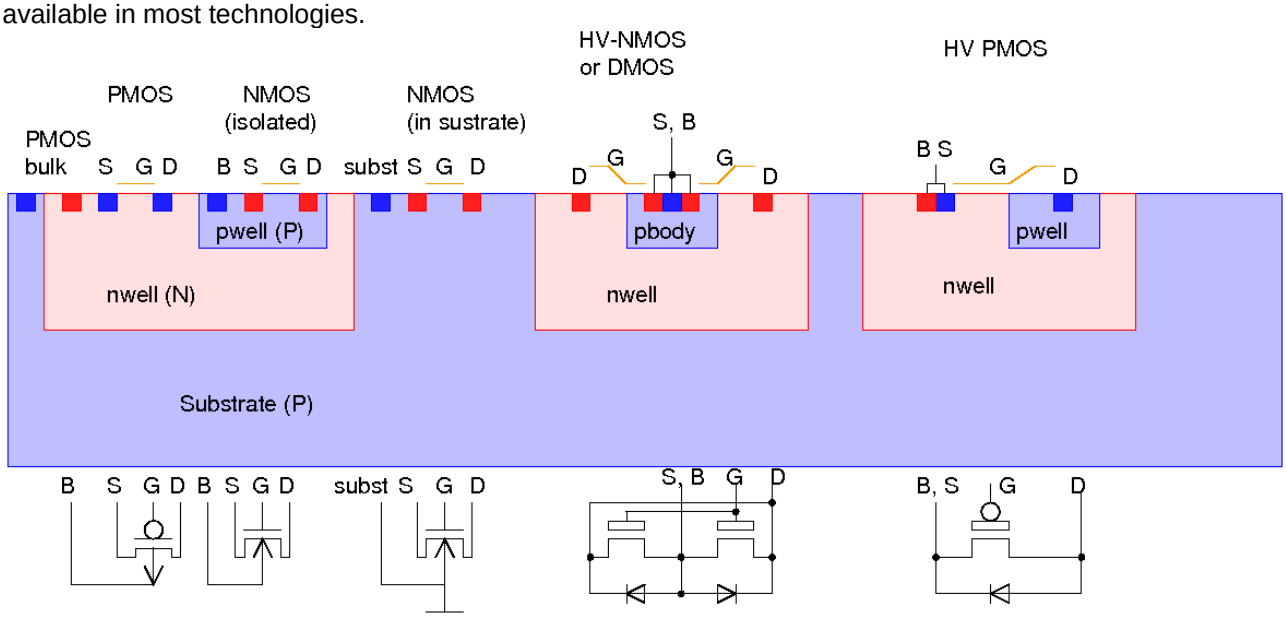

Fig. 1: Typical MOS Transistors in a high voltage technology

Besides MOS transistors all high voltage technologies offer bipolar transistors. Often these transistors are not characterized or only poorly characterized.

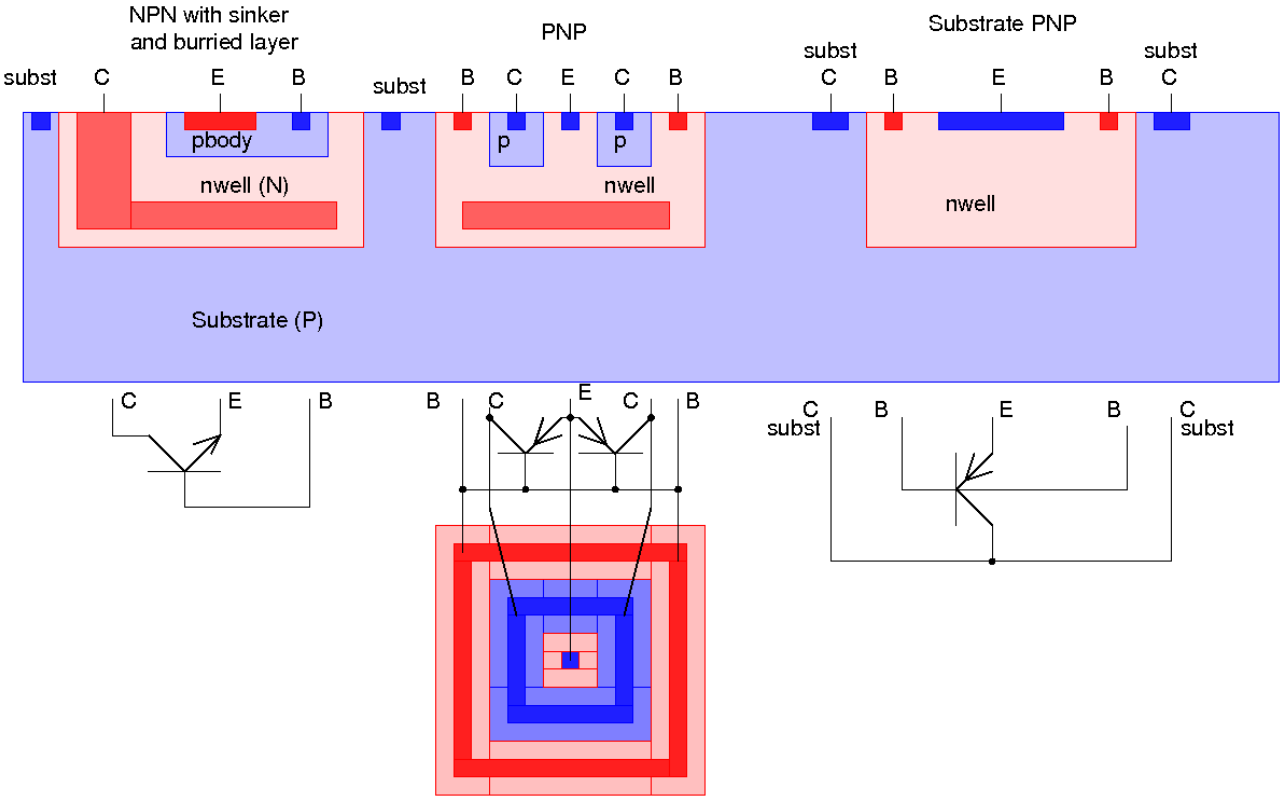

Fig. 2: Typical Bipolar Transistors in a high voltage technology

Besides active components there are passive components and diodes. Most of the passive components include parasitic diodes and / or transistors as well. The following figure gives an overview without showing

too many details.

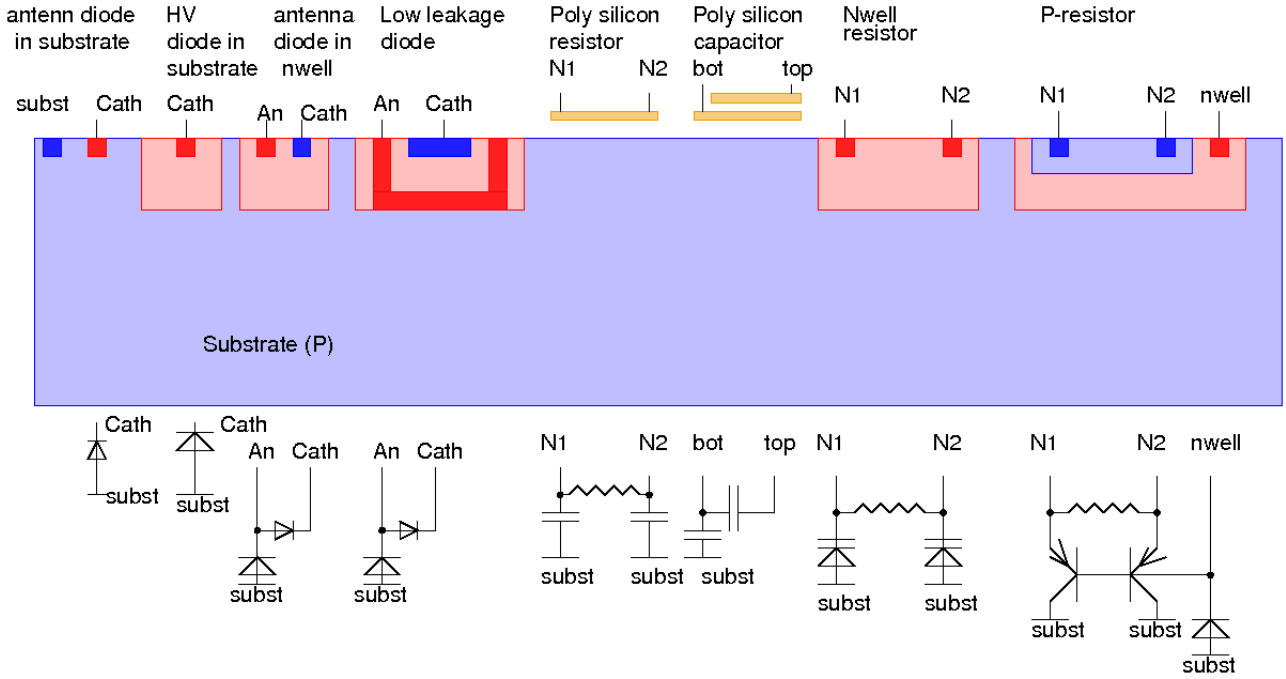

Fig. 3: Passive components and diodes

PMOS Transistors and associated Bulk Parasitics

PMOS transistors are placed in an nwell. Usually this nwell is polarized with a voltage higher or equal to the source potential. So all junctions are blocked in normal operation.

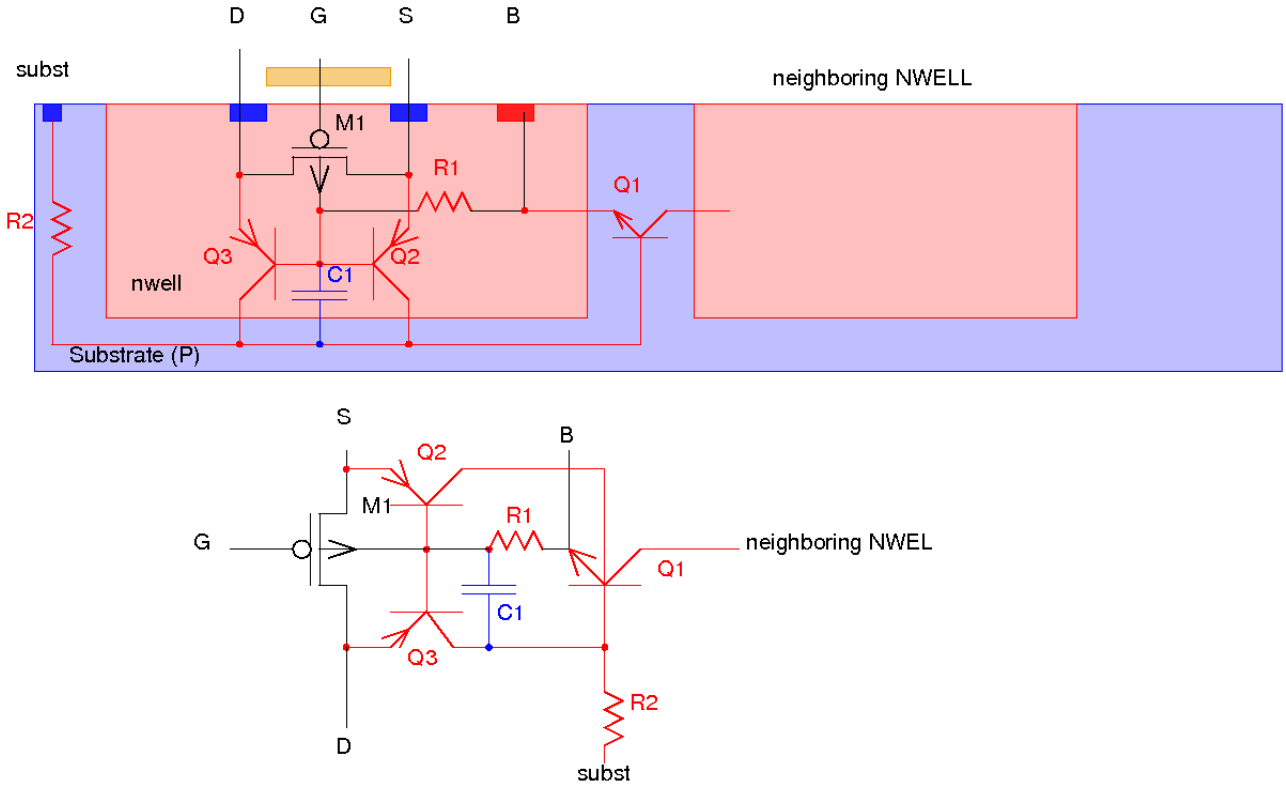

Fig. 4: PMOS transistors

Q1, Q2 and Q3 are inactive in normal operation.

R1 is the resistance between the bulk contact and the area right below the channel. Usually R1 is in the range of some hundred Ohm.
R2 is the resistance of the substrate. Depending on the wafer material R2 is in the range of fractions of an Ohm to some kΩ.
C1 is the junction capacity between the substrate and the nwell the transistor is placed in. C1 can couple substrate noise into the nwell. Due to R1 this noise can modulate the transistor via the back gate.
Q1 becomes active if the nwell potential falls one V_{BE} below substrate potential.
Q2 becomes active if the source potential is one V_{BE} higher than the bulk potential.
Q3 becomes active if the drain potential is one V_{BE} higher than the bulk potential.

Typical Parameters of PMOS parasitics

Componet	High resistive substrate (10Ωcm)	Low resistive substrate (0.01Ωcm)
R1	10Ω to some kΩ	10Ω to some kΩ
R2	about 100Ω to some kΩ	0.2Ω to some Ω
C1	about 100 fF	about 100 fF
Q1	B about 0.1	B about 0.01
Q2	α (I_C/I_E) about 0.1..0.99	α (I_C/I_E) about 0.1..0.9
Q3	α (I_C/I_E) about 0.1..0.99	α (I_C/I_E) about 0.1..0.9

NMOS Transistor in a separate P-well

NMOS transistors can be isolated using pwell inside an nwell. For propper operation the following requirements must be satisfied:

1. pwell potential must be less or equal to drain and source potential.
2. nwell potential must be higher or equal to pwell potential.
3. nwell potential must be higher or equal to substrate potential

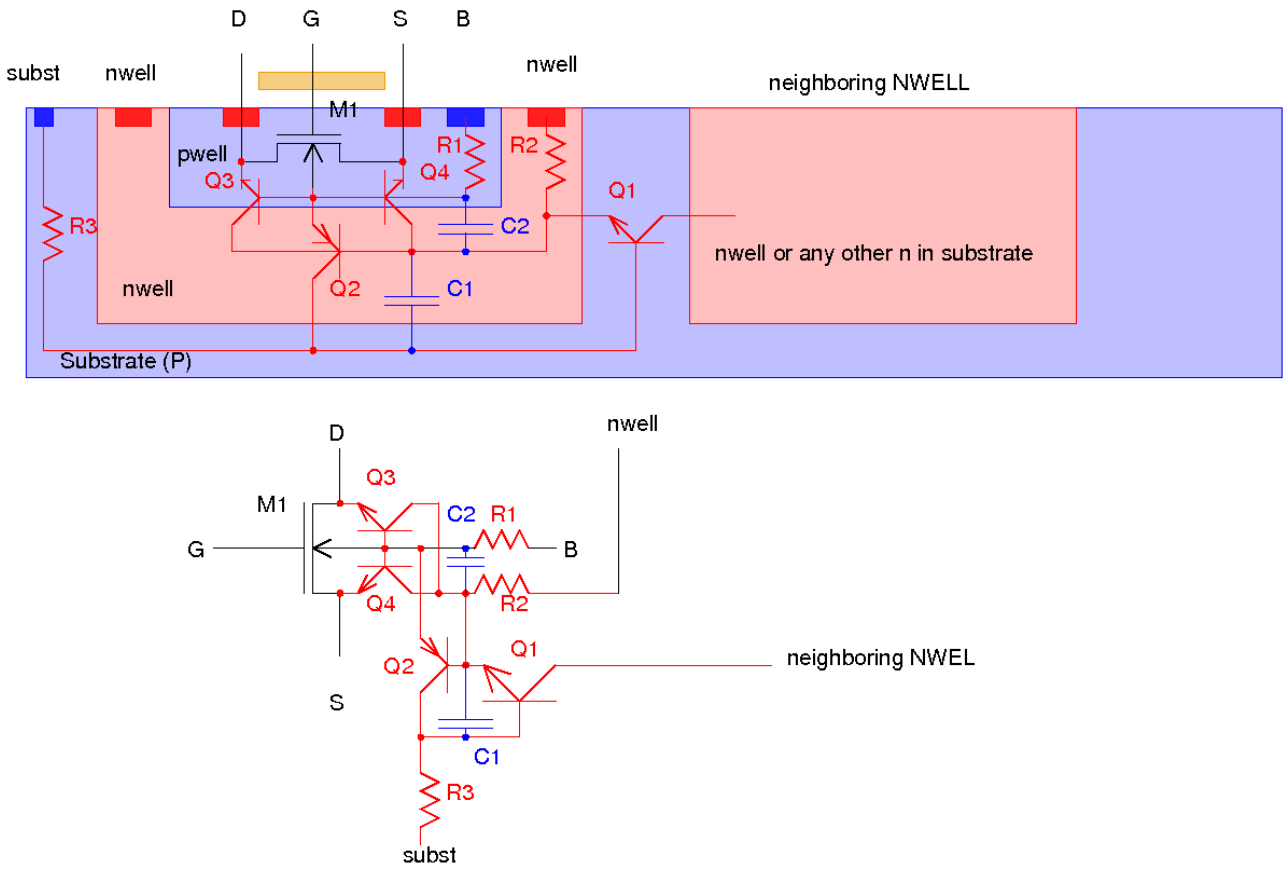

Fig. 5: Cross Section and Bulk Parasitics of the isolated NMOS

Q1 gets activated if the nwell potential falls VBE below substrate potential.
Q2 gets activated if the bulk potential is VBE higher than the nwell potential.
Q3 gets activated if the drain potential is VBE below bulk potential.
Q4 gets activated if the source potential is VBE below bulk potential.

Typical Parameters of isolated NMOS Parasitics

Componet	High resistive substrate (10Ωcm)	Low resistive substrate (0.01Ωcm)
R1	10Ω to some kΩ	10Ω to some kΩ
R2	10Ω to some kΩ	10Ω to some kΩ
R3	about 100Ω to some kΩ	0.2Ω to some Ω
C1	about 100 fF	about 100 fF
C2	about 100 fF	about 100 fF
Q1	B about 0.1	B about 0.01
Q2	α (I_C/I_E) about 0.1..0.99	α (I_C/I_E) about 0.1..0.9
Q3	B about 100 (corresponds	B about 100 (corresponds normal

	normal NPN)	NPN)
Q4	B about 100 (corresponds normal NPN)	B about 100 (corresponds normal NPN)

NMOS transistor in Substrate

NMOS transistors in substrate work correctly as long as substrate is the most negative potential and substrate voltage is constant (without fluctuations, noise, offset versus system ground).

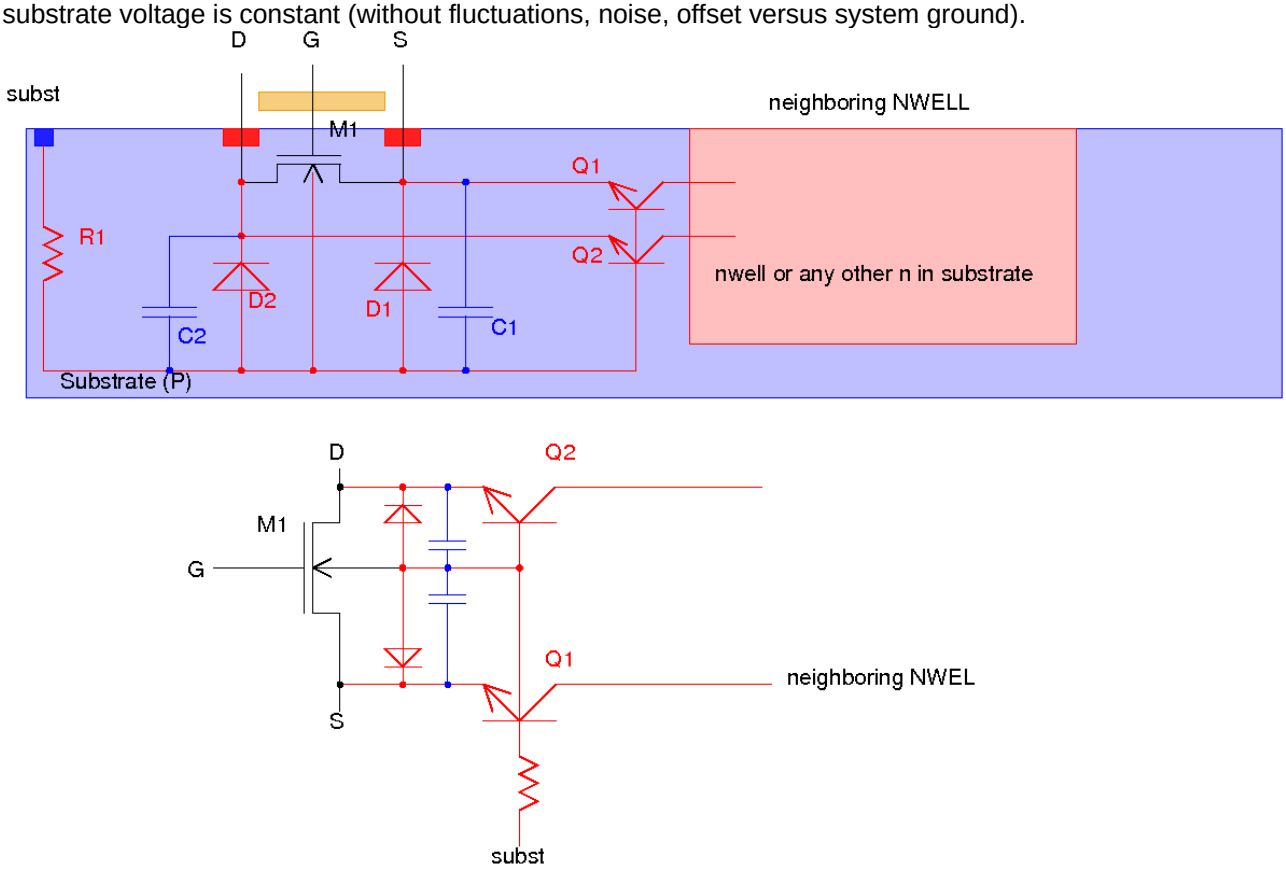

Fig. 6: NMOS transistor in substrate

Parasitic transistors Q1 and Q2 become active if either drain or source is V_{BE} below substrate potential. Capacities C1 and C2 couple switching noise (dV/dt*C) into the substrate. Substrate bounce depends on R1 and inductances of bond wires and pins connecting substrate to the system ground on the board.

Note: NMOS transistors in substrate can cause significant cross talk.

Therefore placing logic transistors in substrate is a hazard in mixed signal design.

Substrate voltage modulates the current flowing through M1 via the back gate.
The transistor embedded in substrate is controlled by two signal inputs: Gate G and substrate subst. The capacitors connecting these two nodes to the inner gate are the oxide capacitiy Cgch and the depletion capacity Cchsub. In most technologies the ratio between Cgch and Cchsub is about:

Cgch / Cchsub = 3

Note: Transistors embeded in substrate amplify substrate noise (Any differential signal between substrate and source) with about 1/3 of the gm of the normal gate G.

Therefore NMOS transistors in substrate are not tolerable for analog design. (If you have analog NMOS in substrate don't worry about noise. It is all messed up anyway!)

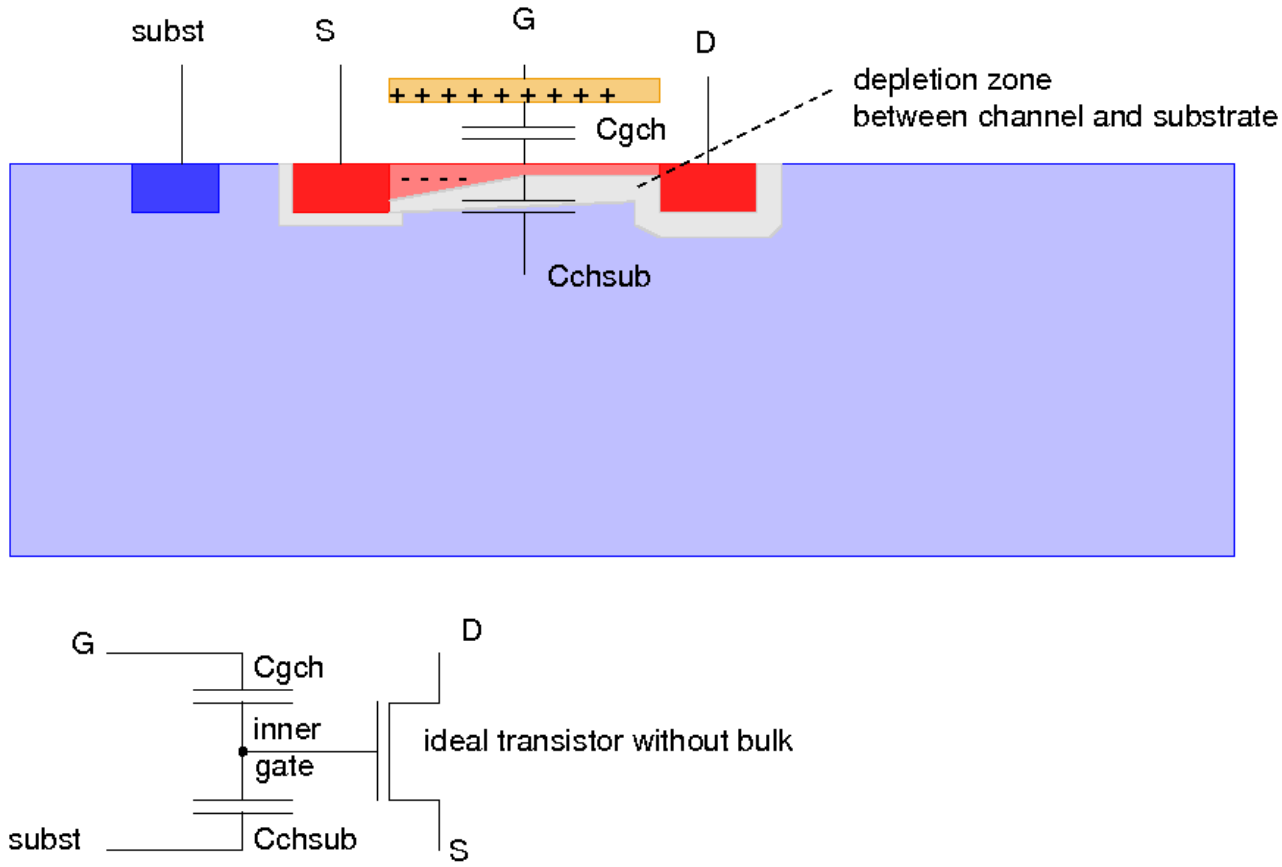

Fig. 7: Backgate influencing transistor performance

HV NMOS and DMOS

High voltage NMOS and DMOS transistors are very similar. In most technologies the only difference is that in a DMOS transistor the channel length is controlled by the out diffusion of the bulk that is implanted through the same mask as the source. (Often the gate poly is used s a mask for both implantations).
Different from a low voltage NMOS the drain is composed of a low doped nwell (required for the electrical field on the drain side of the channel) and an N+ drain contact.

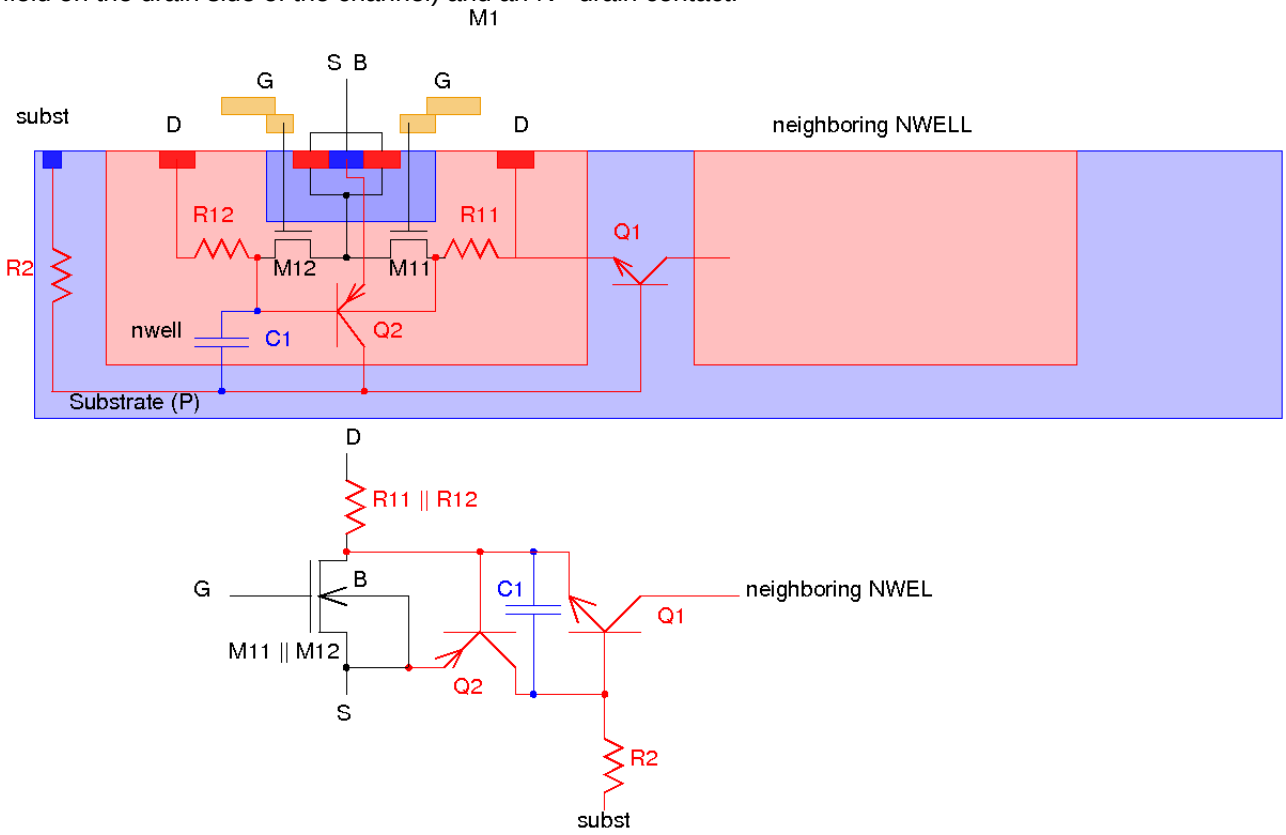

Fig. 8: Cross section of a HVNMOS

For proper function the drain potential must be higher than substrate potential and bulk, source potential must be lower than drain potential.
Q1 becomes active if the drain voltage is V_{BE} below substrate voltage.
Q2 becomes active if the bulpk potential is one V_{BE} higher than drain potential. The gain B of Q2 strongly depends on the burried layer. Some technologies have N-burried (A high N-doping implant at the bottom of the nwell) that makes holes coming from the bulk (acting as an emitter) recombine before reaching the substrate.
C1 is the nwell to substrate capacity. Depending on the size of the transistor C1 ranges from about 0.5pF (minimum device) to some hundred pF (power transistors with 1mm² or more).

Note: The drain of a HVNMOS is capacitively coupled receiver of substrate noise. Fast switching HVNMOS transistors are sources of substrate noise.

Typical parameters of HVNMOS parasitics

Component	without burried layer	with burried layer
R11, R12	minimum device some hundred Ω	minimum device some hundred Ω
C1	minimum device about 0.5pF	minimum device about 0.7pF
R2	some Ω to some kΩ	some Ω to some kΩ
Q1	B about 0.1	B about 0.1
Q2	α (I_C/I_E) about 0.3 to 0.9	α (I_C/I_E) about 0.1 to 0.01

HVPMOS

The high voltage PMOS uses a drain extension to withstand high voltage. The drain extension often uses the pwell mask or similar weak P-dopings. Bulk doping usually is very low. Often the bulk simply is a high voltage nwell.

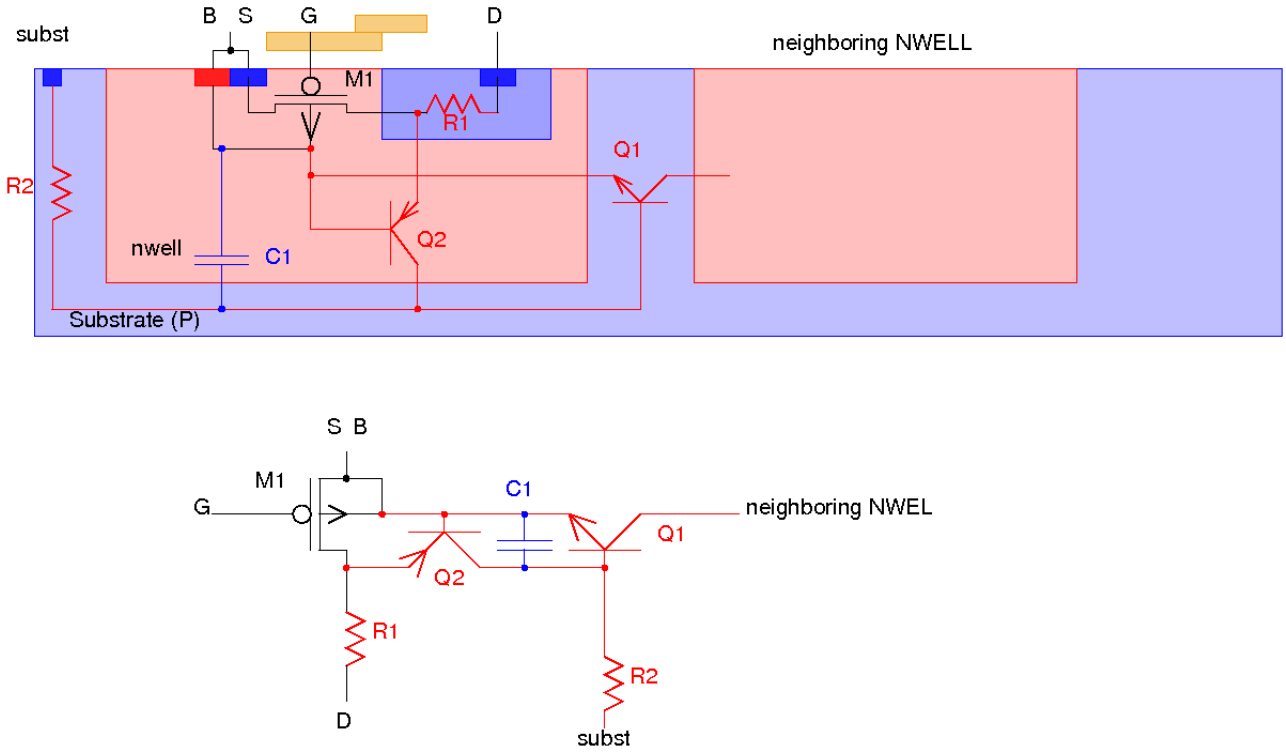

Fig. 9: Cross section of a HVPMOS

The source and bulk are sensitive to RF in the substrate. If the HVPMOS is used as a fast follower C1 can couple RF into the substrate.

Typical parameters of HVPMOS parasitics

Component	without burried layer	with burried layer
R1	minimum device some kΩ	minimum device some kΩ
C1	minimum device about 0.5pF	minimum device about 0.7pF
R2	some Ω to some kΩ	some Ω to some kΩ
Q1	B about 0.1	B about 0.1
Q2	α (I_C/I_E) about 0.3 to 0.9	α (I_C/I_E) about 0.1 to 0.01

NPN transistor

NPN transistors often use pwell or pbody as a base. N-active (the drain of a low voltage NMOS) can be used as emitter. Depending on technology the collector may have a sinker and a burried layer.

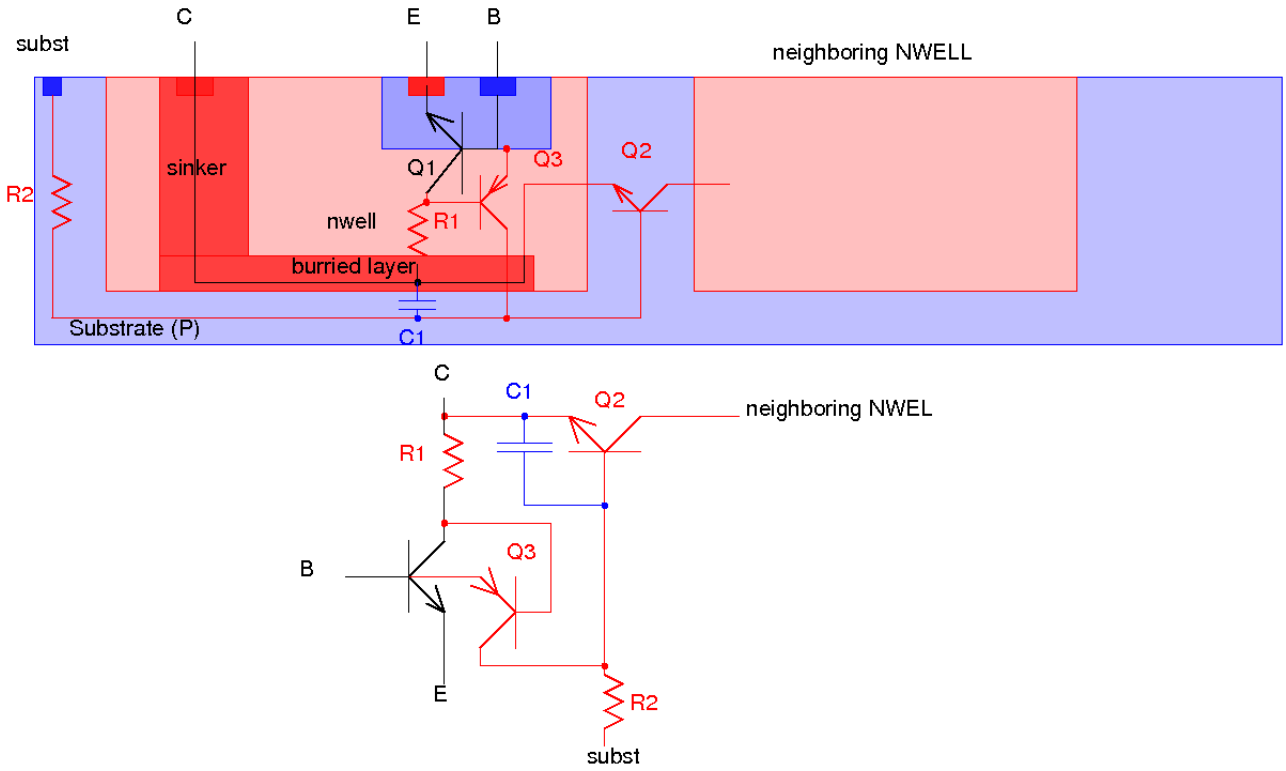

Fig. 10: Cross section of an NPN transistor

The transistor works properly as long as the base potential is less or equal to the collector potential and the collector potential is higher than the substrate potential.

Typical parameters of NPN parasitics

Component	without burried layer	with burried layer
R1	minimum device some hundred Ω	minimum device some 10 Ω
C1	minimum device about 0.5pF	minimum device about 0.7pF
R2	some Ω to some kΩ	some Ω to some kΩ
Q2	B about 0.1	B about 0.1
Q3	α (I_C/I_E) about 0.3 to 0.99	α (I_C/I_E) about 0.1

PNP transistor

Lateral PNP transistors usually only are available in technologies with urried layer. Without purried layer Q3 may well drain much more current to the substrate than the intentional transistor Q11, Q12 carries!

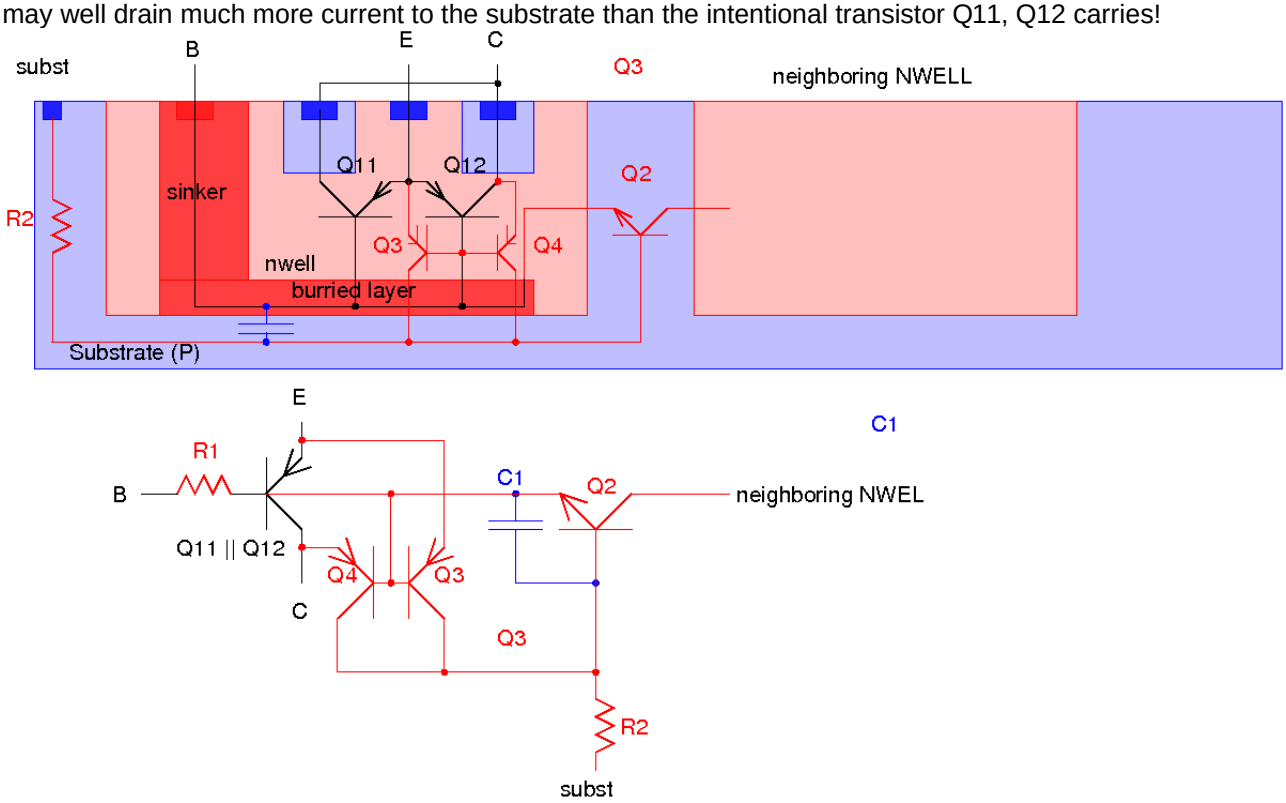

Fig. 11: Cross section of a lateral PNP transistor

Using a burried layer the base resistance R1 can be neglected (it is in the range of 10Ω). C1 is the junction capacity between the base and the substrate. Therefore in mixed signal designs (with substrate noise) PNPs are almost useless.

Typical parameters of PNP parasitics

Component	without burried layer	with burried layer
R1	minimum device some kΩ	minimum device some 10 Ω
C1	minimum device about 0.7pF	minimum device about 0.9pF
R2	some Ω to some kΩ	some Ω to some kΩ
Q2	B about 0.1	B about 0.1
Q3	α (I_C/I_E) about 0.3 to 0.99	α (I_C/I_E) about 0.01..0.1
Q4	α (I_C/I_E) about 0.3 to 0.99	α (I_C/I_E) about 0.1

Substrate PNP

The substrate PNP can only be used as an emitter follower. Almost the complete emitter current is dumped into the substrate. Substrate PNPs can create tremendous substrate noise. If possible PMOS transistors in stead of substrate PNPs should be used.

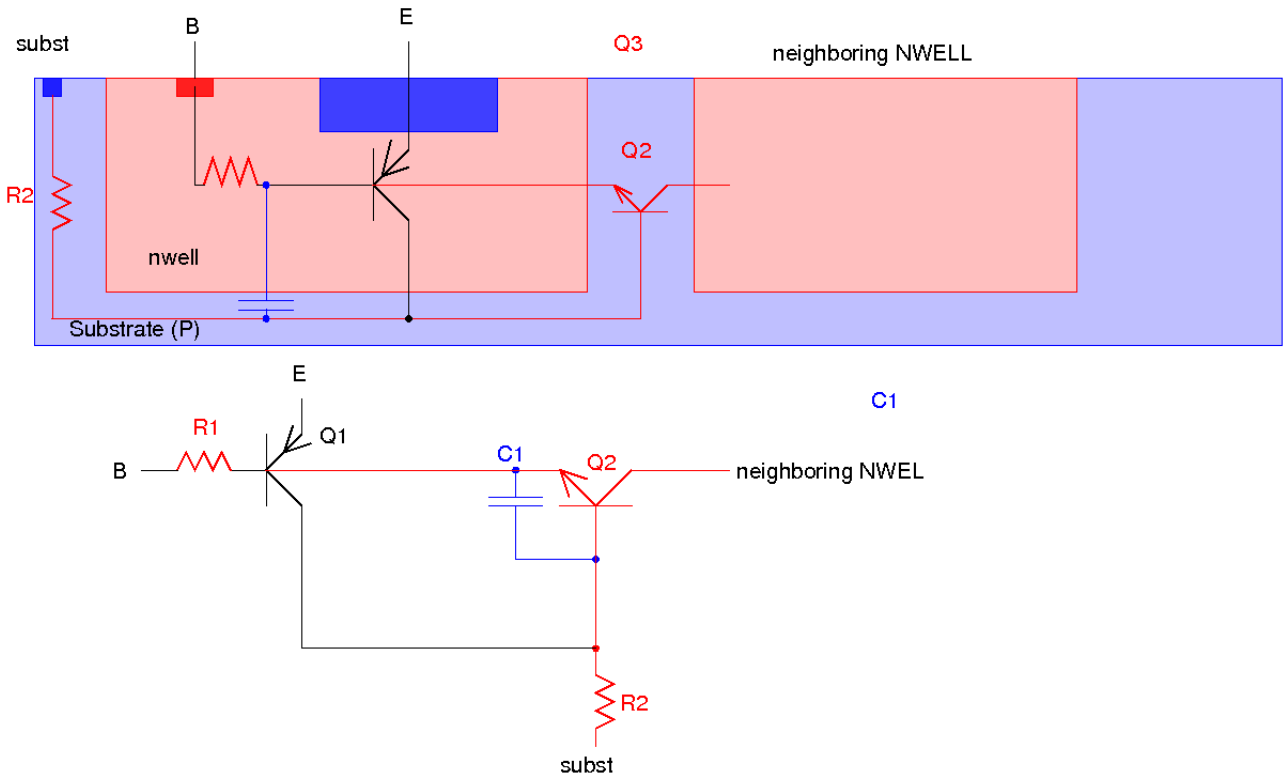

Fig. 12: Cross section of a substrate PNP

Typical parameters of substrate PNP parasitics

Component	without burried layer
R1	minimum device some kΩ
C1	minimum device about 0.5pF
R2	some Ω to some kΩ
Q2	B about 0.1