System Design part 1

September 20, 2019

In the previous posts I showed most of the pieces needed for complex chips. Well I must admit I didn't show much about logic. But that would have been too boring. Since now we have most of the bits and pieces it is time to think about complete systems on chip or in a package.

1 System on a Chip Voltage Classes

Before even thinking of any details we should have a look at voltage classes. In a system on a chip or a system in a package we have a lot of different supply domains. To find an economic solution we first need an rough idea what the voltage means for the design.

1.1 Pure signal processing

As long as we are only doing some signal processing without connecting our chip to such nasty things as cables things are still fairly easy.

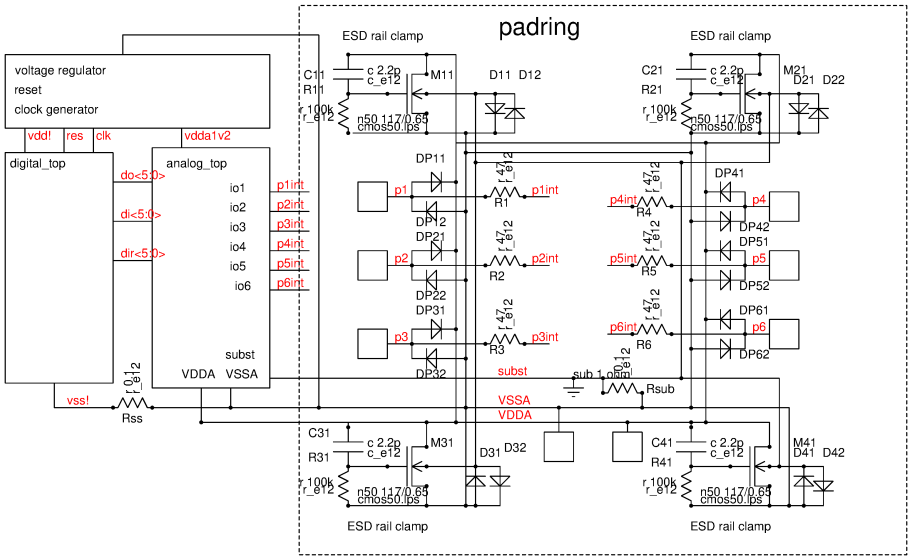

Fig.1.1.1: A simple mixed signal chip

In the simple example shown we only have two supply domains. The logic is supplied by vdd! and vss! . To make things easier global vss! is shorted to the ground net VSSA. VSSA is the ground low resistive ground used for all the input/output circuits (I/Os), the ESD protection and possibly used as an analog ground.

Logic design usually has no concept of a supply voltage. Logic designers love global signals called vdd! and vss! to supply their gates from. This way synthesis becomes easier and supply is SOP (Somebody Other's Problem).

Ideally in the layout vss! and VSSA should be connected right at the pad is a star point - or even better they should use different pins (A pin inductance is a significant impedance as well!). The reason simply is that analog designers are not happy if their reference ground is polluted with digital noise.

VDDA can be something like 1.2V to 1.8V. But this is a bad idea because it forces analog designers to build each amplifier using folded cascodes. That's making things complex and low performant while at the same time current hungry. Choosing VDDA in the range 2.5V to 5V is a much better idea because analog circuits can be built telescopic.

After these very basic considerations we already have a first plan of the supply domains:

supply	voltage	usage
vdd, vss	0.7V to 1.8V	logic, memories
vdda, vssa	2.5V to 5V	analog, IOs, ESD protections

This kind of supply plan can be implemented with almost every technology available on the market.

1.2 Power ICs

As soon as we want to connect a cable (that can be shorted to some higher voltage) or drive inductive loads (motors, switchmode power supplies, solenoids, gate drivers for external power transistors) we need further voltage classes. Which ones we need depends on the specific application.

1.2.1 Server point of load regulators

Blade servers often have a 12V supply rail that is used for switchmode power supplies for the CPUs. Switchmode power supplies often don't need a very complex logic. For robustness reasons the logic may be implemented using 2.5V or 3.3V transistors. The new supply plan may look like this:

supply	voltage	max ratings	usage
vdd, vss	2.5V to 3.3V	4V	logic
vdda, vssa	3.3V to 5V	6.5V	analog, IOs, ESD protections
vddp, vssp	12V (nom)	18V	gate driver stage

A typical technology exactly fitting this requirement is C11HV. The target of such a technology is to offer lateral DMOS transistors with channel lengths around $1\mu m$ and drain extensions to handle up to 18V while at the same time offering a low cost logic. Low cost logic means the feature size (contacts) are still in the 100nm..300nm range to avoid having a complex and expensive mask process.

1.2.2 Laptop Supplies and automotive chips

Laptops usually are supplied from a cable power supply. This cable power supply provides typically 19V. Inside the laptop this voltage must be converted to the supply voltage required by the CPU. The supply plan changes.

supply	voltage	max ratings	usage
vdd, vss	0.7V to 1.8V	4V	logic
vdd2, vss2	2.5V to 3.3V	5V	rugged logic, analog
vdda, vssa	3.3V to 5V	6.5V	analog, IOs, ESD protections
vddp, vssp	19V (nom)	40V (60V)	gate driver stage

Automotive chips require almost the same voltage classes. The vddp domain for automotive chips may need a bit higher maximum ratings. The 1V logic is more needed by the automotive chips than by simple laptop switchmode power supplies.

The technologies are getting more expensive now. Typical examples are BCD9, SPT9, LBC9 or smartmos10. Compare the cost book of a C11HV and one of the other technologies and you will already see a difference.

1.2.3 Mild hybrid applications

Chips used for mild hybrid cars have to operate up to typically 48V with maximum ratings in the range of 100V. Here we approach the limit of system on a chip

approaches. On one side we have to carry the burden of the spacings of 100V while at the same time the Rdson values due to the 100V requirement get worse. On the other side we have to support the feature size of a complex logic.

In other words: Building a 100V power transistor using a technology with feature sizes in the 100nm range becomes very expensive. Paying for a high precision mask set optimized for high density logic while using 50% of the die size for power transistors that are not at all limited by lithography sooner or later makes the design incompeditive.

It might already become more economical to package two chips manufactured in two different technologies in one package than trying to do everything on a single chip. It depends on the number of communication wires between the high voltage domain and the logic is a system on a chip still makes sense.

2 Multi chip systems

Multi chip designs try to avoid the cost of a high density technology on the power side and the cost of the high voltage masks on the logic side. For multi chip systems we need chips with overlapping supply domains.

2.1 Multi chip without galvanic isolation

This is a fairly narrow niche. There are two typical cases:

1. High performance micro controller and high performance analog
2. High performance logic and 100V to 200V power stages

In case 1 the designer wants a cheap but well performing digital processor but can't accept the noise coupling between the digital part of the design and the analog part of the design. (Substrate noise coupling!). Typical examples are delta sigma converters with a resolution down to the μV range in combination with ethernet protocol handlers.

digital chip			analog chip		
supply	voltage	usage	supply	voltage	usage
vddd, vssd	0.8V	CPU			
vddx, vssx	3.3V	I/Os	vddx, vssx	3.3V	I/Os, analog
vdd12, vss12	12V	NVM			
			vbat	12V..40V	regulators

(NVM: Non volatile memory)

The second case often are motor drivers for mild hybrid cars or stepper motor drivers for robotics. There you need the digital performance of a 32bit processor and the power stages for up to 200V.

digital chip			analog chip		
supply	voltage	usage	supply	voltage	usage
vddd, vssd	0.8V	CPU			
vddx, vssx	5V	I/Os	vddx, vssx	5V	I/Os, analog
vdd12, vss12	12V	NVM			
			vbat	50V to 200V	power

2.2 Multi chip with galvanic isolation

Above 200V it usually doesn't make sense to cover the voltage drop with an integrated circuit. Only the power transistors are designed to handle the high voltage. The driver stages float up and down with the source of the power transistor. The input and the output are galvanically isolated.

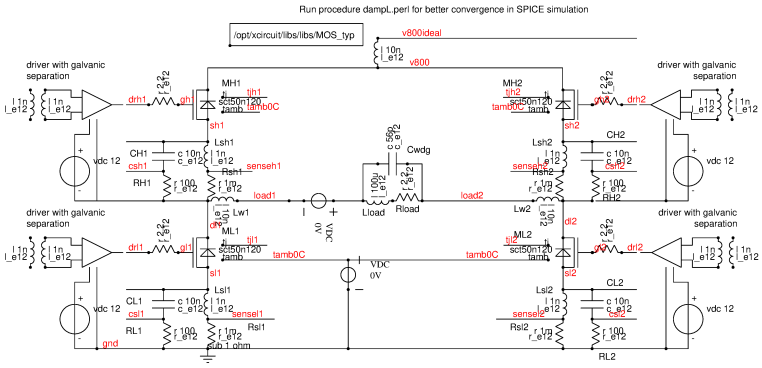

Fig.2.2.1: B4 bridge with galvanic isolation

The circuit shown above displays the concept of a 400V to 800V power bridge. The driver stages each refer to the source of the silicon carbide transistor they drive. Only the power transistors are exposed to up to 1200V (400V to 800V DC plus wire ringing of the load). The driver stages are supplied with 12V to 24V (depending on the gate voltage required. Nevertheless the gate drivers are designed using a 40V technology because the gate wires have an inductance (not shown) that shows ringing of up to 20V (e.g. at rush in shorts the miller capacity of the power transistors will kick back into the driver stage!).

The isolation is provided by the transformers. These transformers may either be on the driver chip itself (Then we need a CVD - Chemical Vapor Deposition - oxide of about 8..10μm) or it can be a separate component. To be able to produce a transformer that can be integrated into an IC package the signal transformer is operated at 500MHz to 1.5GHz (depending on the speed of the technology used). The following figure shows the RF transmitter and the RF receiver.

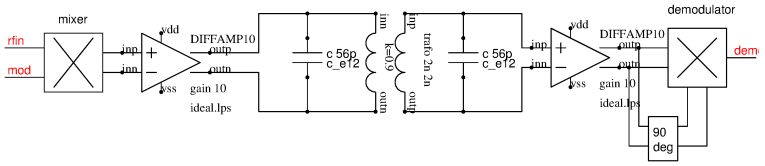

Fig.2.2.2: Driver and receiver of a galvanic decoupling circuit

The components have the following voltage classes:

left (coreless driver)			right (gate driver, receiver)			transformer		
supply	voltage	usage	supply	voltage	usage		DC	pulse
			vddrx	1.2V	RF receiver, mixer			
vddx, vssx	3.3V	amplifier	vddx, vssx	5V	level shifts			
			vddp, vssp	12..40V	SiC driver			
						iso-lation	1kV	6.3kV

Some manufacturers use capacitive couplers instead of transformers. The system voltages however remain similar.

Anyway the transformer also has a significant parasitic capacity. So the coupling has contributions of the magnetic field as well as the electric field. It's more something like an RF wave coupler than a pure transformer.

3 Optical links

As far as I know higher isolation voltages than DC 1kV (pulse 6.3kV) have not yet been implemented in systems in a package using integrated transformers or capacitors. To isolate higher voltages optical links are used. These consist of an LED or a laser diode acting as a signal transmitter, an optical fiber to cover the distance needed to isolate the different parts of the circuit and a photo diode or a photo transistor acting as a receiver.

The biggest problem of optical links is the aging and the production spread of the LED or the laser.

In the 1970s photo-thyristors have been used as well but I have no idea if this technology is still in use.

Using optical links the operating voltage is only limited by the power switch. Single thyristors can handle up to some kV. To design switches for higher voltage several thyristors must be stacked. All thyristors of such a stack must be switched synchronously - a big art!

4 Outlook

Today SiC transistors and IGBTs for up to 1.8kV are commercially available. There are research reports of SiC transistors up to 7kV, but I haven't seen them in pro-

duction yet. SiC transistors for up to 15kV (nominal operating voltage) would be very attractive for railway applications.

GaN transistors can switch faster than SiC transistors. The maximum blocking voltage of commercially available GaN transistors is currently limited to about 400V to 600V. Nevertheless GaN transistors are already in mass production for power supplies of base stations and for server power supplies (converting from line voltage to 12V or 19V)

Theoretically diamond would be a very attractive material as well - but currently it is too expensive. However first research reports of diodes created with doped diamond are already popping up!

Combining high voltage and high current leads to high requirements for circuit protection and thermal management. The real challenges of high voltage power design are on the power side rather than on the digital control. They are in the bare physics. (If you short circuit a modern power transistor you have $1\mu s$ to detect the short and turn off. If you can't make it within that time the transistor will just vaporize!)

Looks like power electronics is just starting now and there will be challenges enough for an other generation of engineers!