# Relaxation Oscillators

August 5, 2019

## 1 Relaxation oscillators

For many integrated circuits a low cost clock source is required. As long as there aren't serial data protocols to be supported simple RC oscillators are preferred for cost reasons. Ring oscillators usually suffer from a wide production spread because the frequency depends on the transistor parameters. Sine wave oscillators usually require highly linear analog amplifiers with a now phase shift in the amplifier. So sine wave oscillators often are current hungry and expensive to build. LC oscillators offer good frequency stability but require external components that again cost money.

Relaxation oscillators try to solve the problem of acceptable accuracy at low cost providing circuits that only depend on very few well controllable components (capacitors, resistors). In terms of frequency stability they usually are somewhere between simple ring oscillators and LC oscillators. For many applications (for instance charge pumps or PWM in the kHz range) this is good enough (Since they are not perfectly stable they even distribute RF emission over a certain bandwidth. This can in certain applications become an advantage. On the other hand RC oscillators always have a certain FM modulation caused by supply fluctuations.)

### 1.1 Astable multivibrator:

The probably best know relaxation oscillator simply consists of only two transistors. This used to be a bread and butter oscillator of the 1960s when transistors still were expensive [3, pages 174ff].

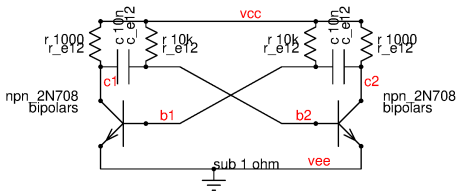


**Fig.1:** Simple relaxation oscillator

The oscillator frequency is determines by the 10K base resistors and the two capacitors. The voltage swing at the collectors runs from the saturation voltage of the transistors ($V_{sat}$) to the supply voltage ($V_{cc}$). The base voltage is limited by

the base-emitter diode. The highest voltage at the base is $V_{be}$. The voltage swing at the base is the same as at the collectors. So the minimum voltage at the base becomes:

$$V_{bemin} = V_{be} - V_{cc} + V_{sat}$$

The voltage drop across the 10K resistors ranges from

$$V_{rmin} = V_{cc} - V_{be}$$

$$V_{rmax} = V_{cc} - V_{bemin} = 2 * V_{cc} - V_{be} - V_{sat}$$

The following simulation shows the signals.

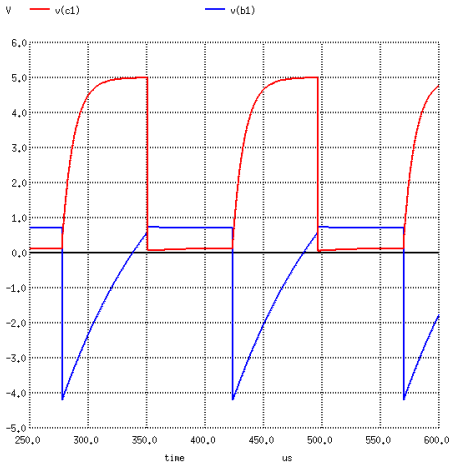


**Fig.2:** Signals of the 2 transistor relaxation oscillator

Now we can calculate the time needed to charge the capacitor from one voltage level to the other (This calculation neglects the base currents and the turn off delay of the transistors!).

$$t_{charge} = R * C * ln(\frac{2 * V_{cc} - V_{be} - V_{sat}}{V_{cc} - V_{be}})$$

The oscillator frequency becomes:

$$f_{osc} = \frac{1}{2 * t_{charge}} = \frac{1}{2 * R * C * ln(\frac{2 * V_{cc} - V_{be} - V_{sat}}{V_{cc} - V_{be}})} \quad (1)$$

In many books the saturation voltage and the base emitter voltage are neglected. For this reason in most of the books you will find:

$$f_{osc} \approx \frac{1}{2 * ln(2) * R * C} \approx \frac{0.7}{R * C} \quad (2)$$

The circuit suffers from several issues:

- The negative peaks at the base limit the supply voltage to about 5V because most transistors have a base-emitter break down of -7V
- The rising edge of the collector voltage is limited by the collector resistors that have to charge the capacitors
- The transistors operate in saturation. This leads to t turn off delay of the bipolar transistors
- Due to the turn off delay the frequency deviates significantly if the circuit is used in the MHz range
- In most technologies turn off delay of saturated bipolar transistors isn't modeled correctly
- The base currents of the transistors slightly change the frequency of the oscillation

In addition this oscillator has the risk of not starting! There is one weak stable operating point: Both transistors are fully on and since they are in saturation the loop gain collapses (This can happen if the base resistors are too low resistive or if the current gain is higher than anticipated). This simple circuit must be verified thoroughly to be sure it starts and operates correctly in all process corners.

### 1.1.1 ECL multivibrator

For high frequencies the following variant of the multi vibrator works better. In this circuit the currents and the voltage swing are limited by the currents sinks I1 and I2.

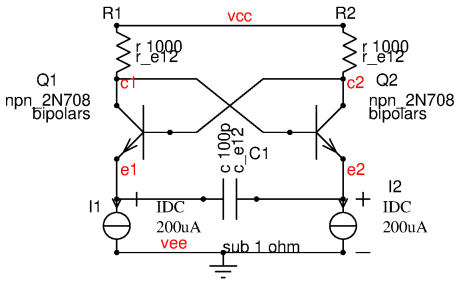


**Fig.3:** ECL relaxation oscillator

The frequency is determined by the capacitor and the resistors R1 and R2. The voltage swing at the resistor is limited by the two current sinks. The current must be limited in a way that the amplitude at the collector remains below Vbe to prevent saturation.

$$V_{dropR} = R_{12} * (I_1 + I_2) < V_{be} - V_{sat} \tag{3}$$

Typically the currents are scaled for a voltage swing of 200mV to 400mV. The charge time of the capacitor becomes

$$t_{charge} = V_{dropR} * C_1 / I_{12}$$

Since the voltage drop follows the current the frequency becomes:

$$f_{osc} = \frac{1}{4 * C_1 * R_{12}} \tag{4}$$

A variation of the current sinks changes the voltage drop over the resistors and at the same time the charge current of the capacitor. This way the currents cancel in the equation.

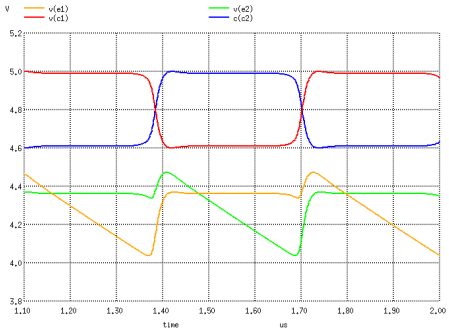


**Fig.4:** Signals of the ECL multivibrator

The little kicks up at each transistor turn off already shows that the practical swing is slightly higher and the real frequency achieved is a little bit lower than the calculated one. So this oscillator isn't too accurate either. The kick up is caused by the charges stored in the transistor before turn off. Nevertheless the achievable high frequency makes it attractive for designing PLLs.

To tune the oscillator either the capacitor or the resistors must be tuned. For high frequency applications replacing the capacitor by a varactor to tune the frequency is a reasonable option. For low frequencies tuning the resistors is required. This can be done replacing the resistors by two PMOS current sources that are intentionally operating in triode region.

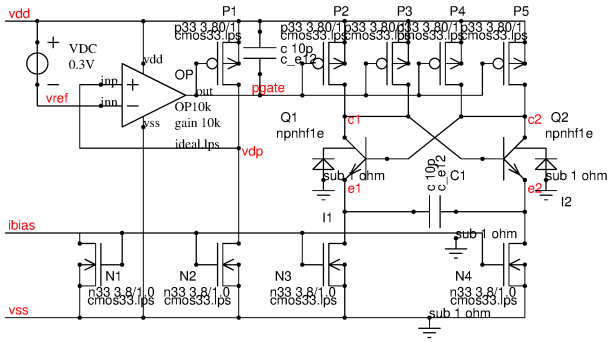


**Fig.5:** ECL multivibrator with tuned resistors

In the circuit shown above the voltage drop over P1 gets regulated to always be 0.3V. Transistor P2 to P5 act as resistors with

$$R_{P2345} = \frac{V_{ref}}{2 * I_{bias}}$$

The resulting frequency becomes

$$f_{osc} = \frac{I_{bias}}{2 * V_{ref} * C_1} \tag{5}$$

To test the circuit the bias current was sweeped

```
ibias vdd ibias pulse 0 100u 0 1m 1m 1m
```

At $100\mu s$ the bias current is $10\mu A$ and the calculated frequency becomes 1.66MHz. At 1ms the calculated frequency becomes 16.6MHz. The simulation shows slightly lower frequencies of 1.4MHz and 11MHz.

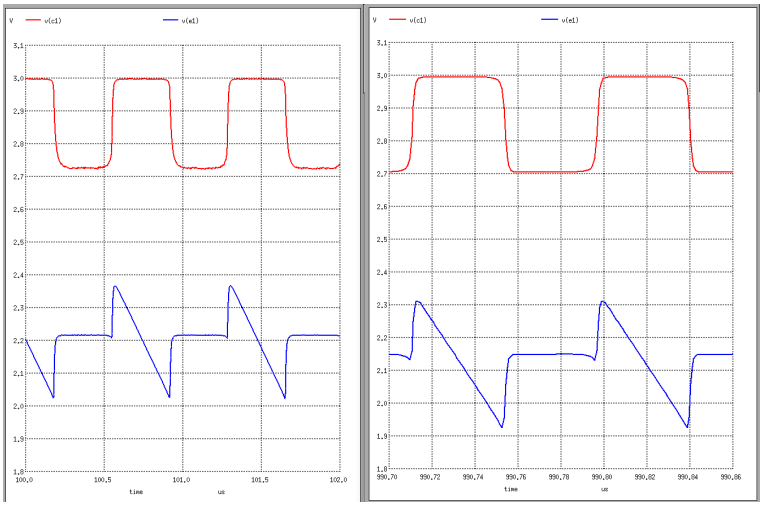

**Fig.6:** Output signals of the oscillator at $10\mu A$bias current and at $100\mu A$bias current

The oscillator intentionally uses bipolar transistors to take benefit of the high transconductance. Replacing Q1 and Q2 by MOS transistors is possible but care must be taken that in all operating corners the following condition is fulfilled:

$$gm > 1/R_{P3456}$$

If this condition is violated the oscillation will stop.

## 1.2 Schmitt Trigger oscillator

The Schmitt trigger oscillator avoids the risk of not starting of the simple 2 transistor multivibrator. There are many variants of using Schmitt triggers for oscillators.

Basically most of them consist of capacitors that are charged or discharged between two levels by a resistor or a current source. Some nice circuits are shown in [1].

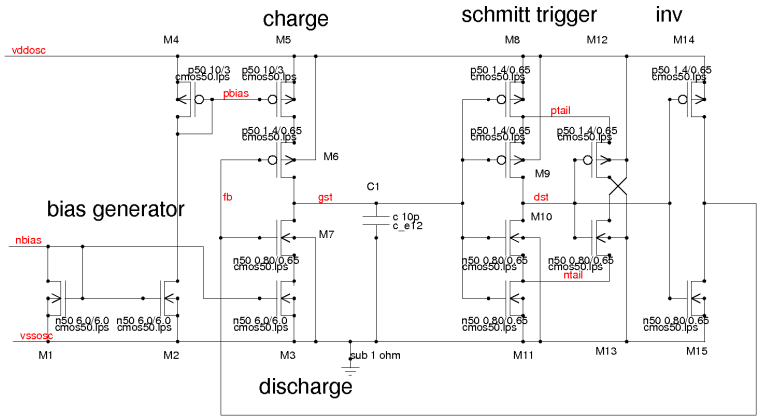


**Fig.7** One example of the oscillator implementations proposed by [1]

Neglecting the propagation time of the schmitt trigger the frequency of this oscillator is a function of the hysteresis Vhyst, the bias current Ibias and the capacity C1.

$$f_{osc} = \frac{I_{bias}}{2 * C_1 * V_{hyst}} \tag{6}$$

The problem is hidden in Vhyst. The hysteresis of the schmitt trigger depends on the supply voltage applied at pin vddosc and on the properties of the transistors M8 to M13. Since 3 of these transistors are PMOS and the other three are NMOS (that do not match!) there is a lot of production spread in the design even if the supply voltage vddosc is kept constant.

**2 Capacitor oscillators:** Mansour Izadinia and Tamas Szepesi show a better solution getting rid of the hysteresis [2]. The price of this solution is that the duty cycle of the oscillator varies with the change of the thresholds of the PMOS and NMOS transistors. The frequency however can be made very stable. The current used must be proportional to the supply voltage. Alternatively the current generators can be replaced by resistors. In this case the cancellation is supply variations is not perfect but still quite good.

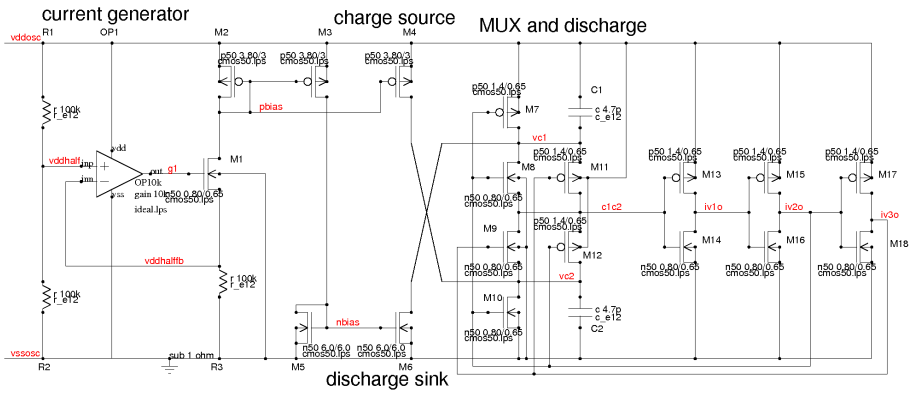


**Fig.8:** Precision oscillator avoiding hysteresis impact on the frequency

The idea of this circuit is that the sum of the charge times of C1 and C2 is constant no matter what is the trip point of the inverter M13, M14. If the trip point is close to vssosc the charge time of C2 gets shorter while the charge time of C1 gets longer by the same amount of time. If the trip pint is close to vddosc charge time of C1 decreases and the charge time of C2 increases. This works well as long as the currents flowing through M6 and M4 are equal and C1=C2=C. Compared to the current flowing in M6 and M4 the resistances of M10 and M7 should be low. (The circuit can be further improved placing additional switches in series with M4 and M6.)

$$f = \frac{R_2}{(R_1 + R_2) * C * R_3} \tag{7}$$

As long as V(c1c2) is below the trip point of M13, M14 signal iv1o is logic 1 turning on M9, M12 and M7. C2 is getting charged by M4 while C1 is shorted by M7. Reaching the trip point the multiplexer switches to C1 turning on M8 and M11. M7 turns off and M10 turns on. Now C2 is shorted and C1 gets pulled down by M6.

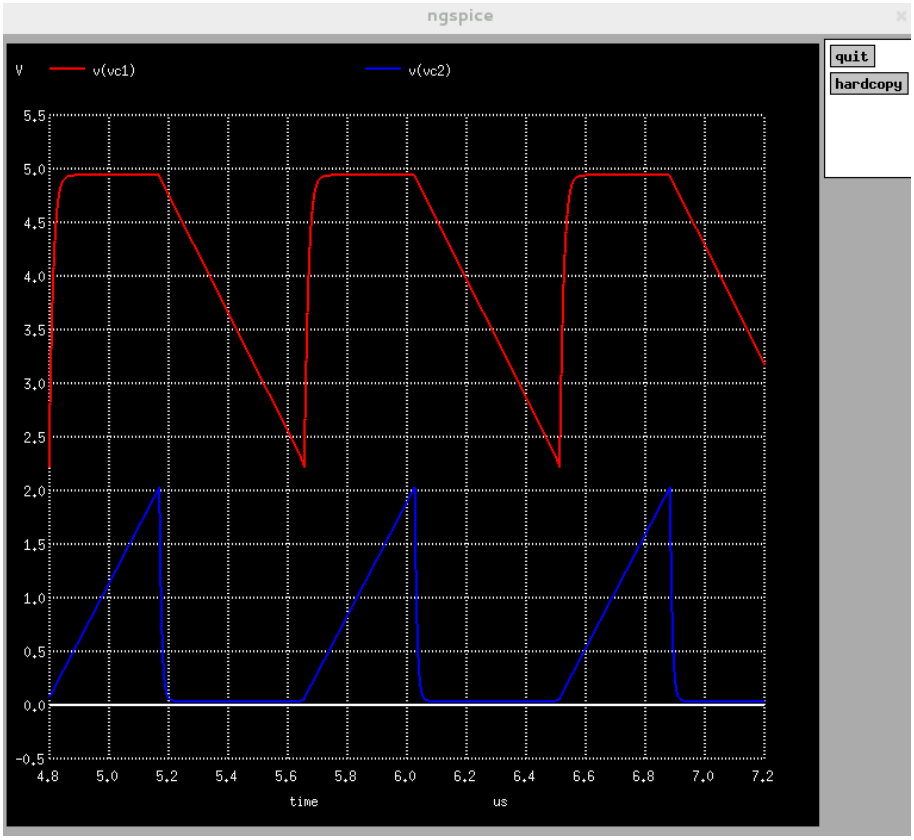


**Fig.9:** Signals at the two capacitors of the oscillator

The inverter used to evaluate the voltage at the timer capacitors is the fastest solution possible (because we add the transconductance of the NMOS transistor M9 and PMOS transistor M8 with a very high current flowing at the trip point). Furthermore the transistor can be made very small without affecting the frequency. So this is probably the relaxation oscillator with the least possible error caused by gate delays and comparator delays. Nevertheless the delays are visible looking at the overshot of the sawtooth signals.

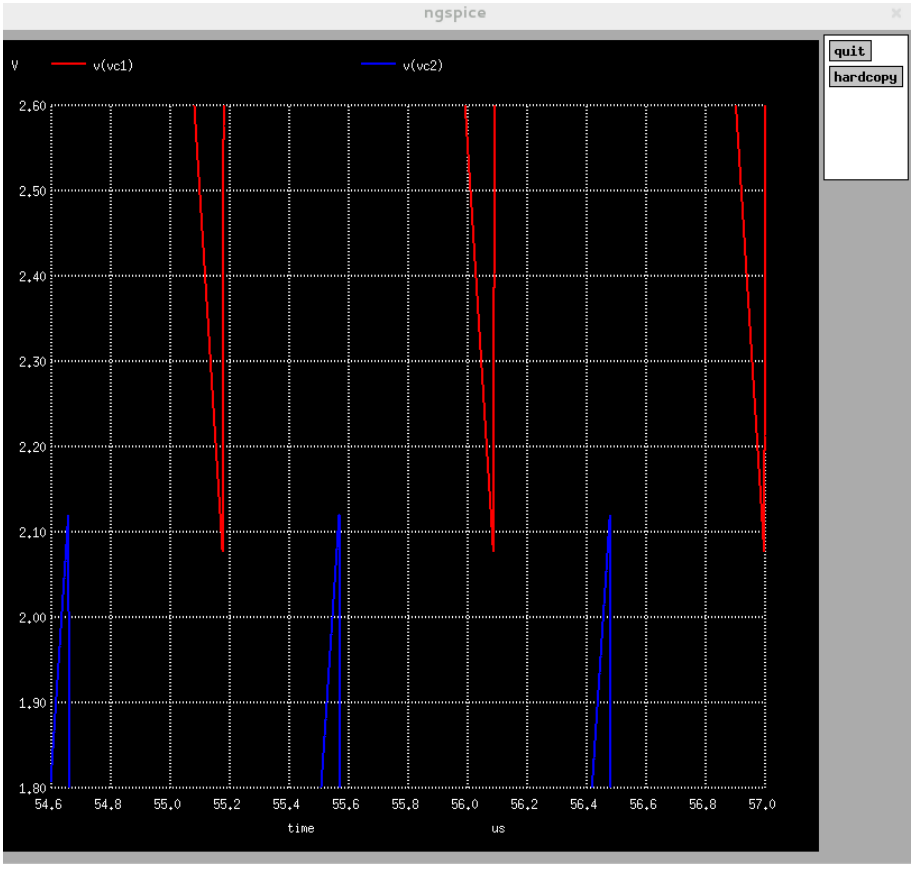


**Fig.10:** Zoom into the trip points. the sum of the overshots is about 20mV.

Compared to a signal swing of 5V (both triangles) the 20mV correspond an error of 0.4%.

### 1.2.1 Calculation of the frequency error caused by the delay of the first amplifier stage

The first amplifier stage in the case shown above is a simple inverter consisting of M13 and M14. It has to drive the capacities associated with the node iv1o. These are the drain capacities of M13 and M14, the gatecapacities of M15 and M16 and the wire capacities of the metal trace connecting the components. The gate capacities of M15 and M16 require special care because there is a capacitiy from the gates to the sources plus a capacity from the gates to the drains. Since signal iv1o has the opposite phase of the gate voltage of M13 and M14 we have to double the drain-gate-capacities of M15 and M16!

$$C_{iv1o} = C_{dM13} + C_{dM14} + C_{wire} + C_{gsM15} + C_{gsM16} + 2 * (C_{gdM15} + C_{gdM16}) \quad (8)$$

The voltage at the output of the inverter starts to change as soon as the input voltage exceeds the threshold of the inverter. The inverter can be linearized for small signals.

$$I_{iv1o}(t) = (V_{c1c2}(t) - V_{th}) * gm \tag{9}$$

In the equation above $V_{th}$is the threshold of the inverter. gm is the transconductance of the inverter exactly at the trip point (The sum of the gm of the NMOS and the gm of the PMOS). Assuming only small overshots the current $I_{iv1o}(t)$can be assumed to be more or less triangular. Assuming the inverter M15, M16 is designed in a reasonable way (threshold in the middle of the supply rails) we can estimate the time needed to charge or discharge the capacity $C_{iv1o}$.

$$\int I_{iv10}(t)dt = C_{iv1o} * \frac{V_{vddosc}}{2} \tag{10}$$

Above the trip point of M13, M14 the current available is:

$$I_{iv1o}(t) = t * \frac{dV_{c1c2}}{dt} * gm \tag{11}$$

with:

$$\frac{dV_{c1c2}}{dt} = f_{ideal} * V_{vddosc} \tag{12}$$

leading to:

$$f_{ideal} * V_{vddosc} * gm * \int tdt = C_{iv1o} * V_{vddosc}/2 \tag{13}$$

Solving the integral the overshot time becomes:

$$t = \sqrt{\frac{C_{iv1o}}{gm * f_{ideal}}} \tag{14}$$

Since the overshot takes place twice per period the total error becomes:

$$t_{error} = 2 * \sqrt{\frac{C_{iv1o}}{gm * f_{ideal}}} \tag{15}$$

Usually we are interested in the relative deviation of the oscillator.

$$err_{rel} = \frac{t_{error}}{T} = 2 * \sqrt{\frac{C_{iv1o} * f_{ideal}}{gm}} \tag{16}$$

Let's have a look at an example:

We want to build a 20MHz oscillator, have an inverter with a gm of 50$\mu$A/V and a capacity $C_{iv1o}$of 20fF.

$$err_{rel} = 17.9\%$$

This means the oscillator is running 17.9% slower than the ideally calculated frequency.

What can we conclude from this result?

1. The supply voltage cancels as long as gm is supply independent (in case of a simple inverter acting as an amplifier this is NOT the case!).
2. the transconductance gm must be made as big as possible. The structure with the highest possible gm versus bias current is the simple inverter.
3. The load of the first inverter stage $C_{iv1o}$must be minimized.
4. The lower we choose the (ideal) frequency the more accurate we can build the oscillator.
5. If we want to build an oscillator with low frequency drift gm must be kept constant over temperature. (So the pure inverter is NOT a good idea because gm of the inverter decreases with temperature.)
6. Fast accurate oscillator will consume a lot of current to provide a high gm of the first amplifier stage.

### 1.2.2 EMC considerations

RF superimposed on the supply will be coupled into the ramp generators M4 and M6. Therefore M4 and M6 should be designed for low Cds (compared to C1 and C2).

## 1.3 Low power relaxation oscillator

Building a low power oscillator high cross conduction currents as in the fast oscillator shown before can not be tolerated. Here the concept is:

1. Move as few nodes as possible
2. avoid static current consumption. Don't use standard comparators with permanently flowing tail currents
3. prevent cross conduction. Don't use logic inverters as amplifiers

One possible solution is shown in the next figure.

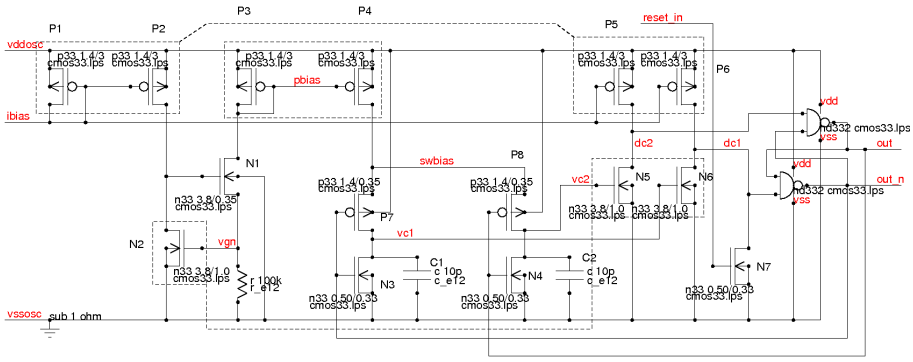


**Fig.11:** Low power oscillator

The oscillator only has four constantly flowing bias paths:

1. ibias flowing through P1.
2. The current producing the charge current flowing through P2 andN2.
3. The reference current corresponding Vth/R flowing through N1 and P3.
4. The charge current flowing through P4 either charging capacitor C1 or capacitor C2.

The currents through P5, N5 and P6, N6 only are active for s short time. Cross conduction in the logic only flows at the instant of switching the latch.

The current charging the capacitor is defined by the threshold of N1.

$$I_{charge} = V_{th}/R \tag{17}$$

The trip point of the amplifiers N5 and N6 correspond their thresholds when the drain current exceeds the current provided by P5 and P6. Since this is the same current N2 is operated at we get the same thresholds. So one charge time is defined by:

$$t_{charge} = C_1 * V_{th}/I_{charge} = C_2 * V_{th}/I_{charge} = C_1 * R = C_2 * R \tag{18}$$

(assuming C1=C2). The ideal oscillation frequency (neglecting the propagation time of the path N5, N6, logic, N3, N4, P7, P8) becomes:

$$f_{osc_{ideal}} = \frac{1}{2 * R * C} \tag{19}$$

Errors caused by the limited speed of N5, N6, P5,P6 can be calculated in a similar way as before.

### 1.3.1 Calculation of the oscillator error caused by delays

Similar to the fast oscillator shown before the amplifier stages N5 and N6 have to discharge the capacities at the drains on N5, P5 and N6, P6. These capacities are the wiring capacity ($C_{wire}$), the drain capacities ($C_{d_{N56}}, C_{d_{P56}}, C_{d_{N7}}$) and the input capacities of the logic gates ($C_{in_{logic}}$).

$$C_{load} = C_{wire} + C_{d_{N6}} + C_{d_{N7}} + C_{d_{P6}} + C_{in_{logic}} \tag{20}$$

Usually these capacities are in the range of some 10fF.

Since we want to have short cross conduction times inside the logic N5 and N6 should be designed for maximum gain. This means N5 and N6 at the trip point should work in the transition zone between weak inversion and strong inversion. (Making N5, N6 bigger leads to necessary capacities, Making N5, N6 too small reduces the ration gm/Id and the switching slopes get slower due to lack of voltage gain.) The assuming weak inversion the gm of N5 and N6 can be calculated:

$$I_d = I_0 * \frac{W}{L} * exp(\frac{k * Vgs_{eff}}{V_t}) \tag{21}$$

$I_0$is a technology dependent factor (can be calculated knowing gate charge, carrier mobility). But since we are interested in gm we don't need it.

$$gm = \frac{dI_d}{dV_{gs}} = I_0 * \frac{W}{L} * exp(\frac{k * Vgs_{eff}}{V_t}) * \frac{k}{V_t} \tag{22}$$

$$gm = I_d * \frac{k}{V_t} \tag{23}$$

Factor k depends on the capacities between the channel and the gate and the capacity between the channel and the bulk. Typical values of k are around 0.7.

$$k = \frac{C_{gate-channel}}{C_{gate-channel} + C_{channel-bulk}} \tag{24}$$

So the estimation for gm becomes:

$$gm = 0.7 * \frac{I_d}{V_t}$$

The rest of the calculation follows the same procedure as done before at the example of the fast oscillator. The subtle difference is hidden in the amplitude of the triangular signals that now follows the threshold $V_{th_{NMOS}}$ of the NMOS transistors.

$$\frac{dV_{c1c2}}{dt} = 2 * f_{ideal} * V_{th_{NMOS}} \tag{25}$$

Assuming the threshold of the logic gates is in the middle of the supply rails this leads to:

$$2 * f_{ideal} * V_{th_{NMOS}} * gm * \int tdt = C_{load} * V_{vddosc}/2 \tag{26}$$

Solving for the delay time we get:

$$t = \sqrt{\frac{C_{load} * V_{vddosc}}{2 * f_{ideal} * V_{th} * gm}} \tag{27}$$

Since this delay takes place twice per oscillator period we can calculate the error time:

$$t_{error} = \sqrt{\frac{C_{load} * V_{vddosc}}{f_{ideal} * V_{th} * gm}} \tag{28}$$

Including the expression for the transconductance gm we get:

$$t_{error} = \sqrt{\frac{C_{load} * V_{vddosc} * V_t}{f_{ideal} * V_{th} * I_d * k}} \tag{29}$$

and the relative error of the frequency:

$$err_{rel} = \sqrt{\frac{C_{load} * V_{vddosc} * V_t * f_{ideal}}{V_{th} * I_d * k}} \tag{30}$$

Let's have a look at an example:

We want to build a 1MHz oscillator, have bias current of N5 and N6 of 1$\mu$A and a capacity $C_{load}$ of the amplifier stages of 20fF. The gm is about 700nA/V. The threshold of the NMOS is about 600mV. For the supply of the oscillator we use 3.3V. The oscillator operates at room temperature and Vt is 26mV.

$$err_{rel} = 4.51\%$$

This means the oscillator is running 4.5% slower than the ideally calculated frequency.

What can we conclude from this result?

1. The load capacity of N5 and N6 must be minimized.
2. The supply voltage should be kept low to minimize the charge to transferred into the load of N5, N6
3. The error follows the square root of the frequency.
4. The error increases with temperature because gm decreases and Vth decreases.
5. If possible use transistors with a high threshold.
6. Scaling to smaller technologies only leads to limited improvements (Cload) because threshold usually are scaled with the supply voltage.
7. Supply the amplifier stages with a ptat current to reduce temperature drift.

### 1.3.2 EMC considerations

The basic concept of the oscillator refers every signal to vssosc. Modulation of the supply voltage vddosc will change the frequency of the oscillator via the early effect of the current generators P4, P5 and P6. This applies to DC changes as well as fast changes of the supply voltage.

Fast changes of the supply voltage can propagate into the ramps of the oscillator via the Cds of P4. To make the oscillator insensitive to RF on the supply the capacity of P4, P5, P6 should be kept as low as possible. (The ratio of Cds of P4 and the oscillator capacitors C1 and C2 is decisive!). The worst case relative pulling range is:

$$\frac{\Delta f_{osc}}{f_{osc}} = \frac{V_{0p} * Cds}{V_{th} * (C + Cds)} \tag{31}$$

In this equation $V_{0p}$ is the peak voltage of the RF on vddosc (measured versus vssosc). $V_{th}$is the trip point of the transistors N5 and N6. Cds is the drain-source (including drain-bulk) capacity of P4. The equation holds the assumption that C1=C2=C.

# References


[1] Stephen K. Michalich, Thomas S. W. Wong, "CMOS schmitt trigger and oscillator", US Patent US4295062, Oct. 13 1981

[2] Mansour Izadinia, Tamas Szepesi, "Precision oscillator circuit", US Patent US4904960, Feb. 27 1990

[3] "Halbleiter Schaltungstechnik", U. Tietze, Ch. Schenk, Springer, 1993