Comparators part 3

July 16, 2019

1 Clocked comparators

Clocked comparators make sense for all kind of applications that are only running while the system clock is available. Typical applications are:

- ADCs
- Synchronized I/Os with voltages deviating from the standard logic 1 and logic 0 levels
- All kinds of sampling systems
- Low power applications with a very slow clock

The benefit of clocked comparators is the high speed of response when the clock is applied. (While there is no clock edge there is no response to changes at all!)

The calculation of the delay of a single gain stage continuous time comparator showed a delay of

$$t_d(V_{od}) = \frac{vdd * C_{mi} * L}{4 * k' * W * (2 * V_{gs0} * V_{od} + V_{od}^2)}$$

for low overdrive voltages. For high overdrive voltages the delay is limited by the bias current of the differential amplifier stage.

$$t_{dmin} = \frac{C_{mi} * vdd}{2 * I_{tail}}$$

Both delays have the factor vdd/2 representing the voltage swing the miller capacity has to be charged or discharged with. A clocked comparator offers the possibility to bring the circuit exactly to the trip point before releasing it to measure the input signal. Ideally the term vdd/2 disappears from the equations. In practical designs there still is some voltage swing required. Speed improvements in practical circuits are in the range of one magnitude over the speed of the corresponding continuous time comparator.

The second option is to temporarily increase the bias current I_{tail}at the sampling event.

For low power applications with long idle time it even is possible to turn off the bias current while the comparator function isn't needed. The bias current only is turned on again some μs before the comparator will be needed and will be turned off again after the measurement.

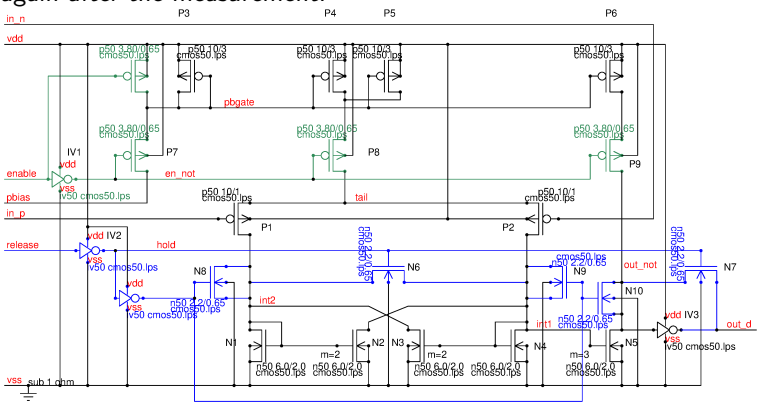

Fig.1: clocked comparator

The comparator shown above is the basic comparator with inherent hysteresis with the following enhancements:

- IV1, P7, P8 can be used to turn off the bias current while the comparator is not in use
- IV2, N6, N7 force the comparator into the equilibrium state before the signal is sampled.
- N8, N9, N10 compensate the charge injection of N6 and N7

At the rising edge of signal release transistor N6 turns off and the hysteresis becomes activated. The nodes int1 and int2 both are at about Vth of transistors N1 to N4. At the same time N7 turns off. The node out_not has an initial voltage that exactly corresponds the threshold of inverter IV3. It will only take fractions of ns until the node out_not will move either above the threshold of IV3 or below the threshold of IV3 after the rising edge of the signal release. N6 must be sized such that the tail current only creates a drop of a few mV over the transistor. The same applies to N7. N7 must be low resistive compared to N5 at the operating point when N6 short circuits the current mirrors N1 to N4. To test the comparator an overtdrive of 5mV was used.

```
vrelease release vss pulse 5 0 5u 1n 1n 2u 20u
vref in_n vss dc 1.23
vin in_p vss dc 1.225
```

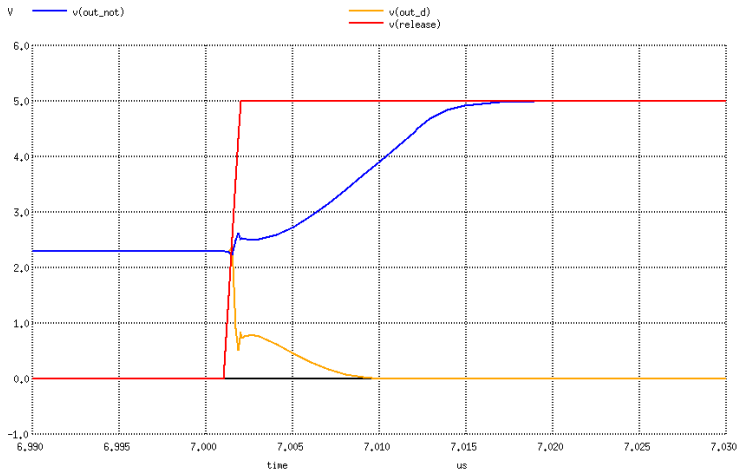

Fig.2: Transient simulation of the clocked comparator

The signal at node out_not shows that the comparator is already at the trip point when the release signal goes up. From the rising edge of signal release to the settling of the comparator it only takes about 10ns using a tail current of $20\mu A$. The hysteresis only is visible in the holding mode of the comparator after about 20ns. Immediately after the rising edge the hysteresis isn't active because the comparator is starting out of the balanced state.

Operating the same comparator in continuous mode the hysteresis becomes visible. The propagation delay increases by factor 4 although the overdrive was increased significantly! (see the last two lines of the stimulus shown below)

```
vdd5 vdd vss dc 5
rbias pbias vss 400k
venable enable vss DC 5
vrelease release vss DC 5
vref in_n vss dc 1.23
vin in_p vss pulse 1.15 1.31 2u 1n 1n 5u 10u
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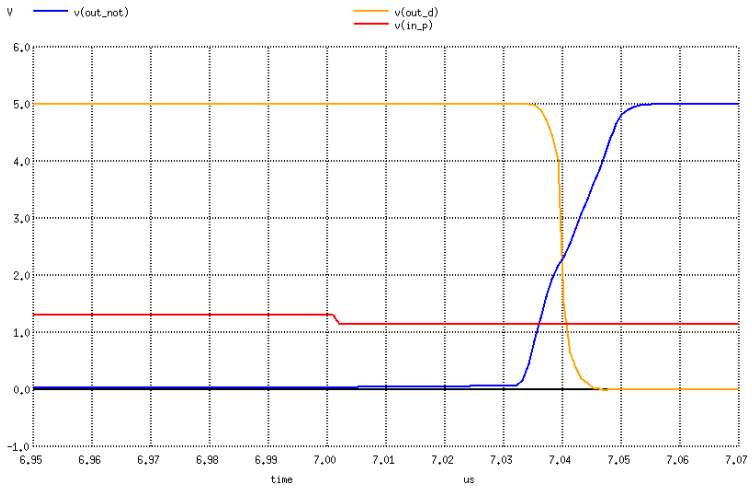

Fig.3: Same simulation as before but the comparator is operated in continuous mode and the input signal is increased significantly

Conclusion: Main differences between clocked comparators and continuous time comparators are:

1. The hysteresis disappears in clocked comparators.
2. The delay from the rising edge of the release signal until the output of the comparator is valid is significantly shorter than the time a continuous mode comparator needs to respond to a change of the input signal.
3. clocked comparators can only be used for systems with the clock running while measurements are taken.

These differences make clocked comparators the preferred solution for ADCs and sampling applications.

1.1 Low supply voltage

Building comparators for low supply voltages leads to similar considerations as building OPAMPs. If classical differential input stages are intended to be used the common mode range decreases reducing the supply voltage. This leads to designs using folded cascodes and rail to rail topologies. Folded cascodes and rail to rail topologies lead to complex circuits and many transistors contributing tho the offset similar to rail to rail amplifiers.

1.1.1 Low cost:

There is one way out of the dilemma: Using a CMOS inverter as an amplifier. CMOS inverters used as linear amplifiers have a poor power supply rejection of only

bout 6dB. Therefore using inverters as linear amplifiers requires a very stable supply voltage. The following circuit shows the concept.

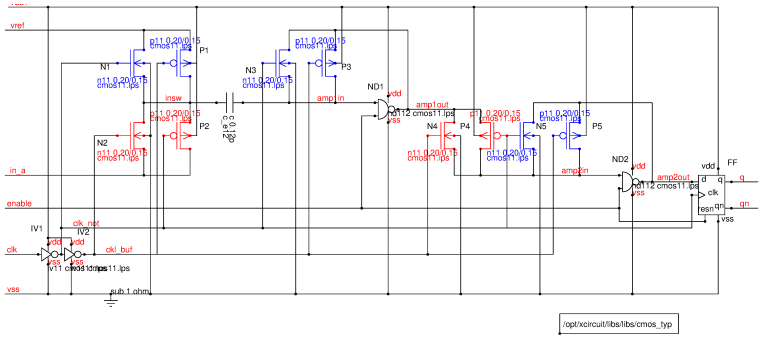

Fig.4: NAND gates used as amplifiers for a comparator

The amplifier has 2 operating states. In one state the reference voltage vref is measured. During the reference measurement the blue colored transistors are on. Both NAND gates are shorted between the output and the input. The voltage of the node amp1in is exactly the equilibrium voltage. The difference between this equilibrium voltage and the reference vref is stored in the 100fF capacitor. To measure the input voltage the blue switches are opened and the red switches are closed. If the input voltage at in_a is higher than the reference the node amp1in moves up and both inverters amplify the signal. The output amp2out moves changes to HIGH. If the input voltage at node in_a is lower than the reference the node amp1in moves down and output amp2out becomes LOW.

Switches N4 and P4 can also be replaced by a capacitor. This is advantageous if the operating points of the two gates ND1 and ND2 differs significantly while the switches N3, P3 and N5, P5 are closed. On the other hand the size of a capacitor is bigger than the size of the two minimum transistors N4, P4. It is a trade off between offset and chip real estate.

At the falling edge of the clock the result of the measurement is stored in the flip flop FF.

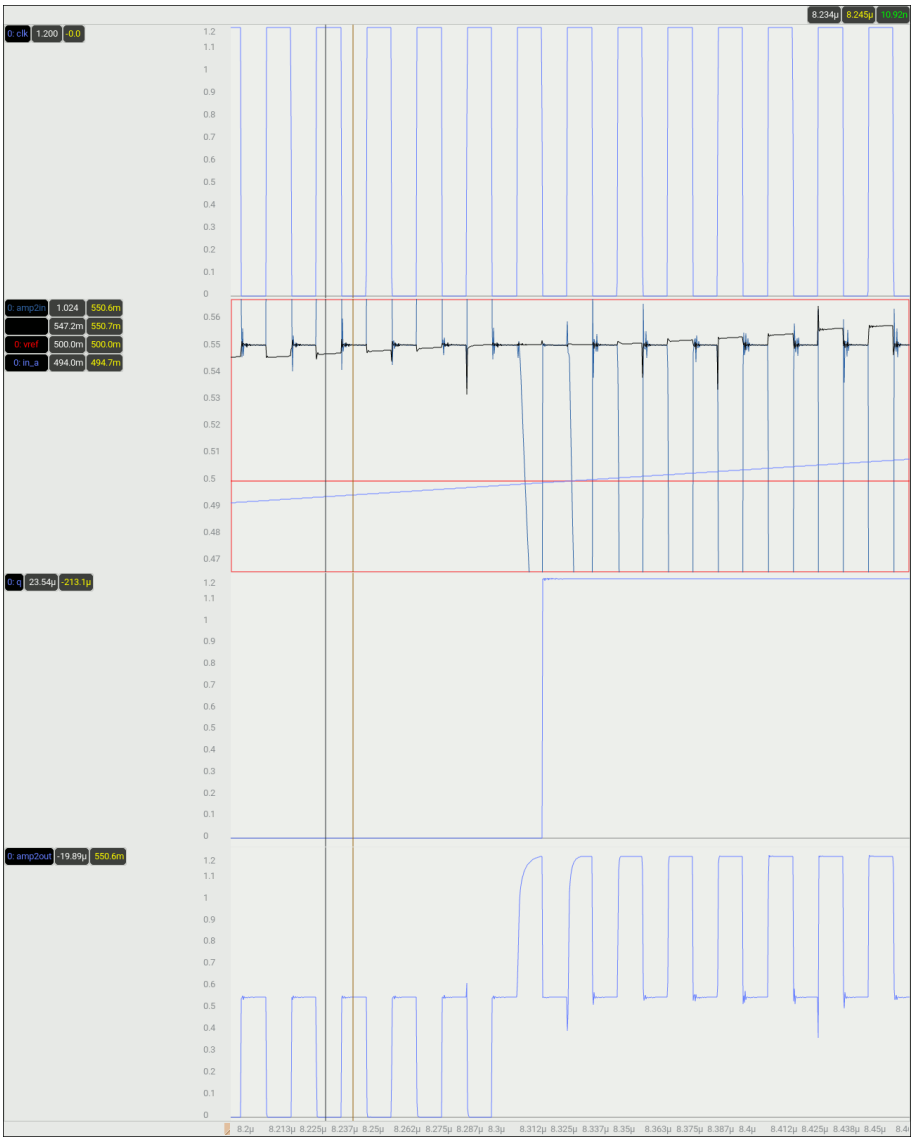

Fig.5: Simulation of the clocked comparator using 2 NAND gates

In the second strip the increasing voltage V(in_a) (blue) and the reference V(vref) (red) is shown. The signal is amplified by the two NAND gates while the clock signal is logic 1. The output amp2out toggles either between 0 and the equilibrium voltage (V(in_a)<V(vref)) or between 1 and the equilibrium voltage (V(in_a)>V(vref)). The flip flop samples the state of amp2out at every falling edge of the clock.

The performance of the circuit is limited by the clock feed through of the switches into the capacitor. There are several options to improve the circuit:

- Use same size NMOS and PMOS transistors to compensate the clock feed

through

- Add dummy transistors of half the size of the switches connected to the opposite phase of the clock to compensate clock injection
- Increase the capacity to reduce the clock injection

2 Summary

Now we have seen the concept of clocking comparators and one possible low cost solution for low supply voltage. Besides these two extremes there are many more possible implementation. Each implementation has it's own pros and cons.

Building clocked comparators certain things should be kept in mind no way how the details are done:

1. Clocked comparators in most cases are significantly faster than their continuous time look alike.
2. Most clocked comparators have no hysteresis because we always start from an equilibium point to achieve the high speed.
3. No clock no signal.
4. Clocked comparators are sampling systems. Input signals close to the clock frequency (or it's harmonics) will be folded down to the base band!
5. Clocked comparators may have undefined states at the output if the input signal exactly crosses the threshold at the clock edge.
6. Even single buffering as shown in figure 4 doesn't provide security. The flip flop may start to oscillate if the signal changes exactly at the clock edge. Consider double buffering for critical applications.
7. Capacitor coupled clocked comparators sometimes offer offset cancellation for free.
8. If simple inverters are used as amplifiers the PSRR is only about 6dB