Comparators part 2

July 4, 2019

1 Propagation delay of a comparator

The circuit shown in my last post is a nice example to demonstrated the change of the comparator delay with the overdrive. The overdrive is the voltage the input signal exceeds the threshold. For a better understanding what happens lets replace the ideal amplifier by a transistor level design. The replacement is in the dashed box.

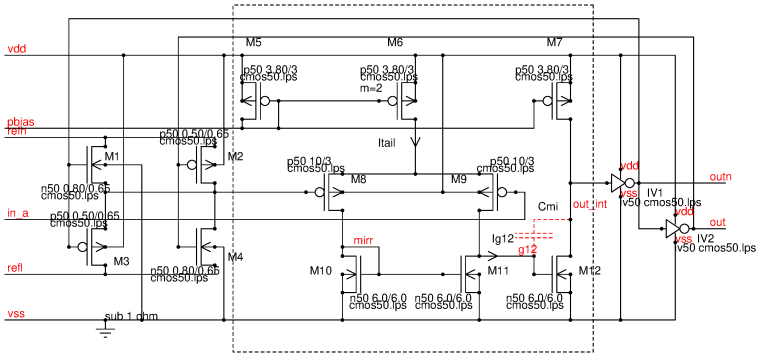

Fig.1: Replacing the ideal amplifier with a transistor level circuit

The miller capacity Cmi is the most important capacity limiting the speed of the comparator. Cmi is a parasitic capacity (between the drain and the gate of M12). This is why it is drawn dashed.

To flip the hysteresis the node out_int must either be charged from 0V to about vdd/2 (rising edge) or from vdd down to vdd/2 (falling edge). The time needed to charge the capacity Cmi is the dominant delay of the comparator. charging time becomes

$$t_{charge} \approx \frac{C_{mi} * vdd}{2 * I_{g12}} \tag{1}$$

The capacity Cmi is non linear. This is why the equation holds a $\approx$ instead of a $=$ sign. To get a feeling what happens we can calculate with some kind of an average capacity.

The current driving the node g12 is the difference between the drain current of M9 and the drain current of M8. Exactly at the trip point both currents are equal

and the comparator will be infinitely slow. As soon as the signal at node in_a drops slightly below refl the current through M9 exceeds the current flowing through M8. This difference depends on the voltage difference between refl and in_a and the transconductance of the differential amplifier M8, M9.

Vice versa if the voltage if in_a is slightly higher than the voltage of refh the current through M8 will exceed the current through M9.

The minimum delay is reached when either M8 or M9 takes over the complete tail current Itail. Neglecting the propagation delay of the two inverters we get:

$$t_{dmin} = \frac{C_{mi} * vdd}{2 * I_{tail}} \tag{2}$$

The current through M8 and M9 is determined by the gate voltage of the transistore, the aspect ratio and the technology parameter k'. (k' depends on thee oxide thickness and the carrier mobility)

$$I_d = k' * \frac{W}{L} * V_{gseff}^2$$

With $V_{gseff} = V_{gs} - V_{th}$and $k' = \mu\varepsilon_{sio_2}/2nt_{ox}$, n=1.2..1.6. At the equilibrium point M8 and M9 both carry the same current. the resulting gate overdrive at this point becomes:

$$V_{gs0} = \sqrt{\frac{I_{tail} * L}{2 * k' * W}} \tag{3}$$

or reordered:

$$I_{tail} = 2 * k' * \frac{W}{L} * V_{gs0}^2$$

The gate voltage for other operation points can be described by this equilibrium voltage and an overdrive voltage V_{od}.

$$V_{gseff} = V_{gs0} + V_{od} \tag{4}$$

The tail current must always match the sum of the currents through M8 and M9. The output current charging or discharging the parasitic capacity Cmi is the difference of these two currents.

$$I_{tail} = I_{M8} + I_{M9} \tag{5}$$

$$I_{g12} = I_{M9} - I_{M8} \tag{6}$$

The current through M8 can be replaced by the current through M9 leading to

$$I_{g12} = 2 * I_{M9} - I_{tail} \tag{7}$$

Describing the current through M9 by the equilibrium voltage and the overdrive yields

$$I_{g12} = 2 * k' * \frac{W}{L} * (V_{gs0} + V_{od})^2 - I_{tail}$$

$$I_{g12} = 2 * k' * \frac{W}{L} * (V_{gs0}^2 + 2 * V_{gs0} * V_{od} + V_{od}^2) - I_{tail}$$

This simplifies to

$$I_{g12} = 2 * k' * \frac{W}{L} * (2 * V_{gs0} * V_{od} + V_{od}^2) \tag{8}$$

Since the current through M8 and M9 can only range from 0 to the tail current the overdrive voltage is limited to the following range

$$V_{od_{min}} = 0 \tag{9}$$

The minimum case means there is no current charging or discharging Cmi and the delay becomes infinite.

The maximum case means the complete tail current is flowing into the capacitor.

$$I_{g12} = I_{tail} = 2 * k' * \frac{W}{L} * V_{gs0}^2$$

Combining the equations:

$$2 * k' * \frac{W}{L} * V_{gs0}^2 = 2 * k' * \frac{W}{L} * (2 * V_{gs0} * V_{od} + V_{od}^2)$$

Solving for V_{od}yields

$$V_{od_{1/2}} = V_{gs0} * (-1 \pm \sqrt{2})$$

Since we defined out overdrive as positive the valid solution is

$$V_{od_{max}} = V_{gs0} * (\sqrt{2} - 1) \tag{10}$$

Higher overdrive voltages won't make the comparator any faster because the complete tail current already flows through one of the two transistors. The delay time for overdrive voltages below $V_{od_{max}}$will lead to a delay time of

$$t_d(V_{od}) = \frac{vdd * C_{mi} * L}{4 * k' * W * (2 * V_{gs0} * V_{od} + V_{od}^2)} \tag{11}$$

This looks like a complex equation while the accuracy of the result is limited by the poor knowledge of the average capacity Cm1. The big benefit of this equation is that now we can clearly see which design parameter has which influence on the delay of the comparator. The following plot displays the comparator delay versus the overdrive voltage for tail currents $1\mu A$and $10\mu A$.

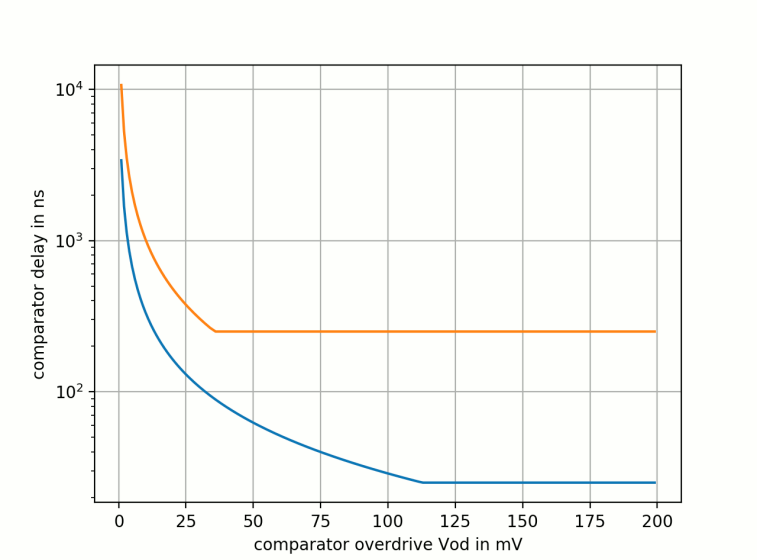

Fig.2: Comparator delay versus overdrive voltage for tail currents $1\mu A$(orange) and $10\mu A$ (blue).

Each of the curves has two ranges. Below $V_{od_{max}}$ the delay is dominated by the transconductance of the differential stage and the overdrive voltage. Above $V_{od_{max}}$ the delay is determined by the tail current alone. On the left side of the knee separating the two ranges the differential stage operates in a more or less linear way. On the right side of the knee the differential stage can be regarded as a switch that simply switches the tail current to the miller capacity or to the current mirror diode. The knee itself moves to the right increasing the tail current (as long as we leave the aspect ratio of the differential stage untouched).

For high performance comparators (for instance used in ADCs) we typically want to have the knee as far to the left as possible and the tail current as high as we can afford. This means the aspect ratio W/L must be scaled with the tail current according to the application. This works as long as the differential pair operates in strong inversion. Moving the knee down to less than about 20mV isn't possible because the input stage approaches weak inversion then. Since we can only push the knee to the left in a limited way the design of ADCs with an LSB of less than about 25mV (8 Bit at 5V supply) either has to be paid by a significant reduction of speed or we have to consider more complex multi stage comparators with a limited output swing of the first stage. (So the first stage can operate with a low overdrive similar to a linear RF amplifier while the 2nd stage operates with an overdrive in the 50mV range again to switch the output transistor.)

The calculations of equation (11) reducing everything to the miller capacity Cmi and the current charging or discharging the gate of M12 is a rough simplification because the miller capacity is voltage dependent. Nevertheless we can see which design parameter propagates into the circuit performance in which way.

Since the overdrive voltage is limited to less than V_{gs0} the dominating part of the denominator is the factor $2 * V_{gs0} * V_{od}$.The propagation delay approximately follows

$$t_d(V_{od}) \sim \frac{1}{V_{od}}$$

The following relations show which circuit change has the highest impact on the speed of the comparator:

$$t_d \sim vdd$$

$$t_d \sim C_{mi}$$

for low overdrive voltages (left side of the knee):

$$t_d(V_{od}) \sim \frac{L}{W}$$

If the overdrive is high (right side of the knee) the aspect ratio of the differential stage doesn't matter anymore:

$$t_{d_{min}} \sim \frac{1}{I_{tail}}$$

Knowing these propagations we can see much better which optimization has the best effect than simply designing by try and error and simulating with SPICE or SPECTRE.