Comparators part 1

July 1, 2019

Comparators are used to interface the analog signals with the logic. Analog signals can be characterized by a voltage. In most cases the signal can range from 0V to the supply rail.

Digital input require discrete signal levels. Either 0V plus some tolerance (corresponding a logic 0) or supply minus some tolerance (vdd corresponding a logic 1). Signals between the levels representing a logic 1 or a logic 0 aren't permitted.

The purpose of a comparator is to assign every analog signal below a certain threshold to a logic 0 and above the threshold to a logic 1.

1 Types of Comparators

Comparators can operate continuous time or time discrete.

Continuous time means any change of the input will be reported to the output almost immediately (Of course there is a certain propagation delay). The change of the output will occur asynchronous to the clock of the logic.

Time discrete comparators only change state when a clock signal is applied. The output changes synchronous with the system clock.

1.1 Schmitt Trigger circuits

Schmitt trigger circuits usually have an inherently defined threshold. The don't need a reference. Some schmitt triggers use the supply voltage itself as a reference.

2 Fields of use

Each of the concepts (time continuous, time discrete, Schmitt trigger) has a specific field of usage.

2.1 Use of continuous time comparators

Continuous time operation is required in situations the comparator function must be available while the system clock isn't running. Typical applications are:

- Under voltage detection

- Reset circuits
- Wake up inputs
- relaxation oscillators
- protection functions that have to take the system to a save state immediately, even if the logic isn't clocked

The continuous time comparator is biased permanently. The required bias current depends on the speed requirements.

2.2 Use of time discrete comparators

Time discrete comparators sample the input signal at each clock edge. Typical applications are:

- ADCs (Analog Digital Converters)
- Slow protections that are only needed while the clock is running
- I/Os that only need to be monitored while the logic is clocked

Time discrete comparators only need to be biased during signal acquisation. While the comparator is inactive the bias currents can be turned off to reduce current consumption. During the signal acquisation even high bias currents to reduce the propagation delay can be used without much penalty regarding the average current consumption of the chip.

Many of the basic circuits of clocked (time discrete) comparators are identical with the continuous operating comparators. The only enhancement versus the continuous time comparator is the switching of the bias current and the setting of an initial operating point right before the acquisation takes place.

2.3 Use of Schmitt triggers

Schmitt triggers have an inherent generation of the trip points. Usually they also feature a hysteresis. Typical applications are:

- Bandgap OK detection
- noise removal at digital inputs
- They can be part of a comparator to shape the signals

3 How to build a comparator

A comparator can simply be designed using an operational amplifier in an open loop configuration. We just need the OPAMP and a reference voltage determining the threshold.

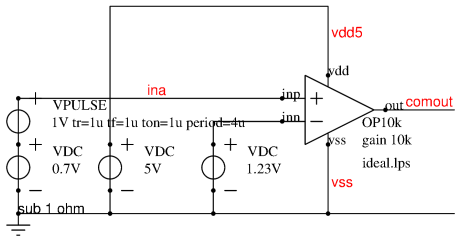

Fig.1: The most simple way of building a comparator

The comparator shown has a threshold of 1.23V. The input signal at node ina swings from 0.7V to 1.7V.

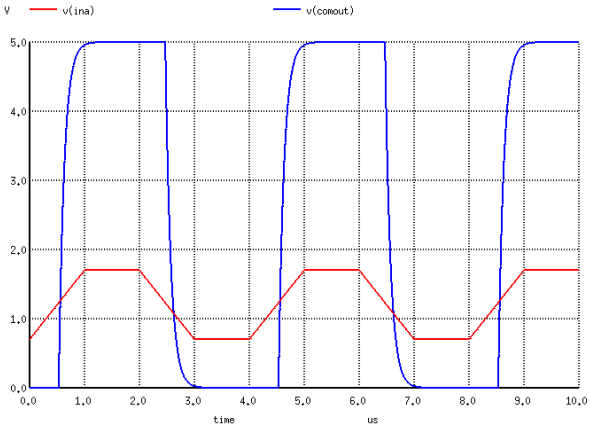

Fig.2: Simulation of the most simple comparator

The simulation already discloses some weaknesses of this simple design:

1. Using an OPAMP with limited slew rate leads slow switching edges
2. If the logic reads the signal during the edge the result of the logic operation becomes undetermined. Even worse: some logic circuits such as flip flops might oscillate if signal levels between 0 and 1 are applied
3. If the input signal (red) were superimposed with noise we would see multiple edges instead of one clean edge.

To improve the situation the following actions usually are to be taken:

1. Add a hysteresis to the circuit to make it less noise sensitive.
2. remove the frequency compensation to make the switching edges faster.
3. Add a schmitt trigger between the comparator and the logic to further speed up the edges.

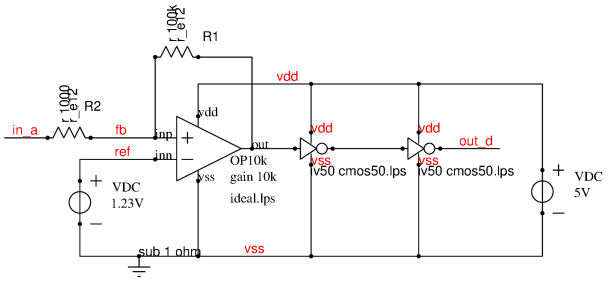

Fig.2: Comparator with hysteresis and buffers to make the switching edges faster.

The output of the analog amplifier can be 0V or vdd. The ratio of the resistors R1 and R2 and the reference applied at node ref determine the trip points.

Let's assume we have a ramp from 0V to 5V applied at pin in_a. The output out_d will change from 1 to 0 when the voltage at node fb crosses 1.23V (the reference voltage applied at pin ref). Due to the divider R1 and R2 and the initial output voltage of 0V this will happen when the voltage at in_a crosses:

$$V_{tripH} = V(ref) * \frac{R1 + R2}{R1} \tag{1}$$

In the above example this happens at $V_{tripH} = 1.01 * 1.23V = 1.2423V$.

Next step let us assume we have a falling ramp from 5V to 0V. Since we are starting from a high level the initial voltage at he output out_d is equal V(vdd). This increases the voltage at node fb.

$$V(fb) = V_{in} * (1 - \frac{R2}{R1 + R2}) + vdd * \frac{R2}{R1 + R2} \tag{2}$$

The trip point for the falling edge becomes:

$$V_{tripL} = V_{ref} + \frac{R2}{R1} * (V_{ref} - vdd) \tag{3}$$

In our example this falling trip point calculates as $V_{tripL} = 1.23V + 0.01 * (1.23V - 5V) = 1.1923V$.

Well, in this simplified calculation we assumed the gain of the amplifier to be much higher than the ratio $\frac{R1}{R2}$. This is a simplification that will not contribute too much error as long as the gain of the amplifier is at least 2 magnitudes higher than the resistor ratio.

The difference of the trip points $V_{tripH}$and $V_{tripL}$is called the hysteresis of the comparator.

$$V_{hyst} = V_{tripH} - V_{tripL} = \frac{R2}{R1} * vdd \tag{4}$$

The following plots show the simulated performance.

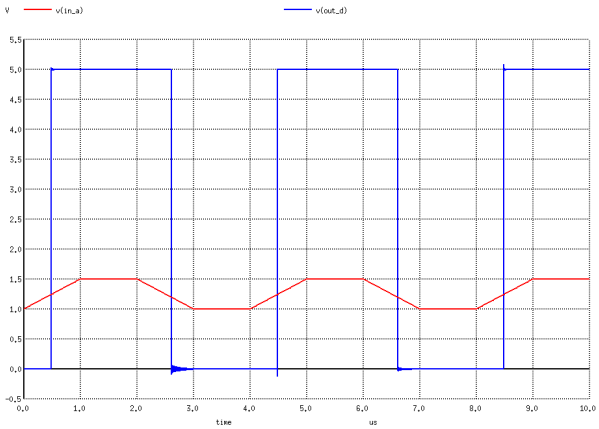

Fig.3: Simulation of the comparator with hysteresis and buffers to drive the logic

To better see the hysteresis let's zoom in a bit:

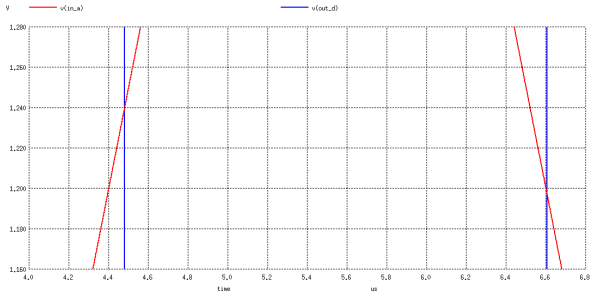

Fig.4: Zooming Y to see the hysteresis

The hysteresis found is close to the expected values calculated before. The rising and the falling edge at the outputs mainly is determined by the speed of the inverters. Since in the test setup there is no load capacity on wire out_d the edges we see are only limited by the capacities of the transistors in the inverters. With long traces on the chip the speed of these nodes can be about one magnitude slower!

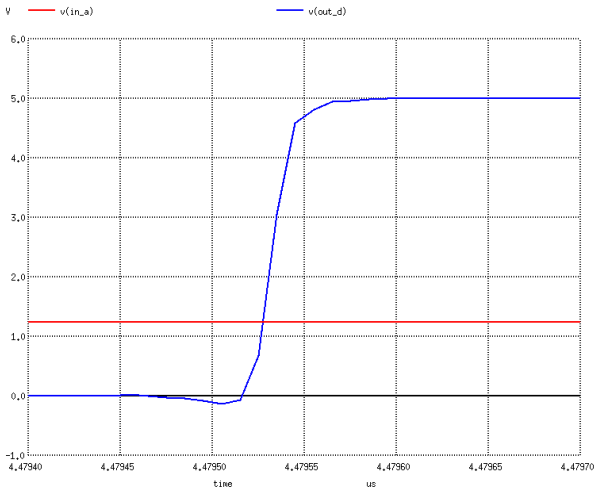

Fig.5: One of the switching edges of the comparator with buffer

The simple topology shown here has the disadvantage that the positive input has to provide the current for the resistor network R1 and R2. If the source driving in_a is high resistive the source resistance must be added to R2. So the source resistance changes the hysteresis and the trip points!

A second disadvantage is the dependence of the trip points on the supply voltage. To overcome these draw backs other topologies are used in practical design.

3.1 precision comparator with two amplifiers

Using two amplifiers is a standard approach for precision designs. One of the first implementations was the famous 555. Now there is no more static kick back into the input of the comparator. What remains is a capacitive kick back into signal in_a caused by the miller capacities of the input transistors of the two amplifiers. The trip points no are determined by the reference voltage and the resistor divider R1 to R3.

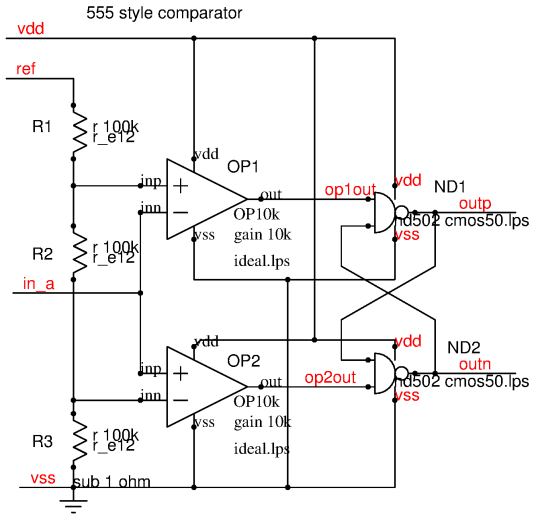

Fig.6: Precision comparator with two amplifiers

In case of the original NE555 of 1971 [1] the nodes ref and supply vdd are shorted internally. The original NE555 used a bipolar input stage. So deviating from ideal there still in an input current flowing into the base of the differential transistor bases. But this current is already several magnitudes lower than the current flowing through R1 and R2 of the conceptual implementation shown before.

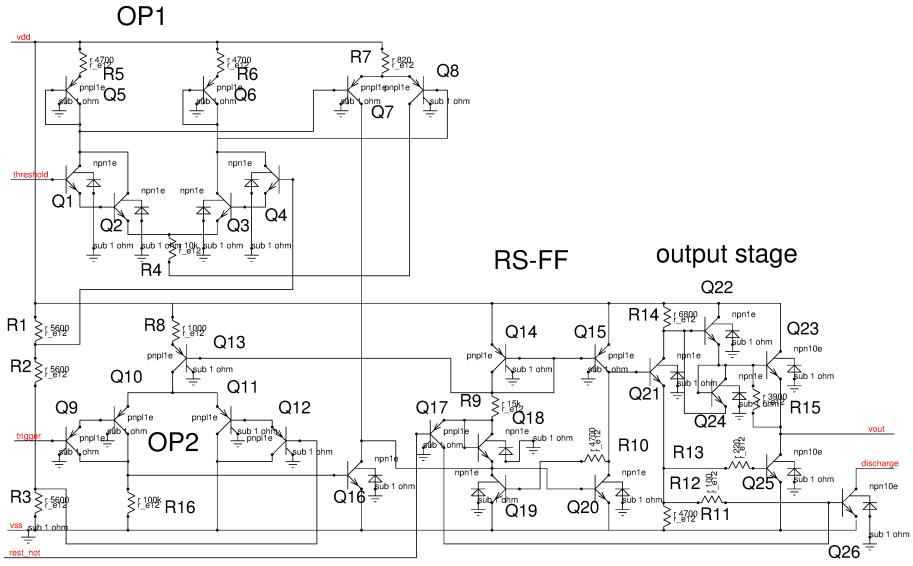

Fig.7: Original NE555 circuit

The 555 still is in production but the transistor level implementation has changed a lot using more modern technologies. (Today there are variants on the market using

the classical bipolar implementation as well as variants using CMOS implementations).

3.1.1 Cost reduction

Building two amplifiers in stead of one consumes more silicon real estate than necessary. The following circuit eliminates one of the expensive amplifiers by switching the reference.

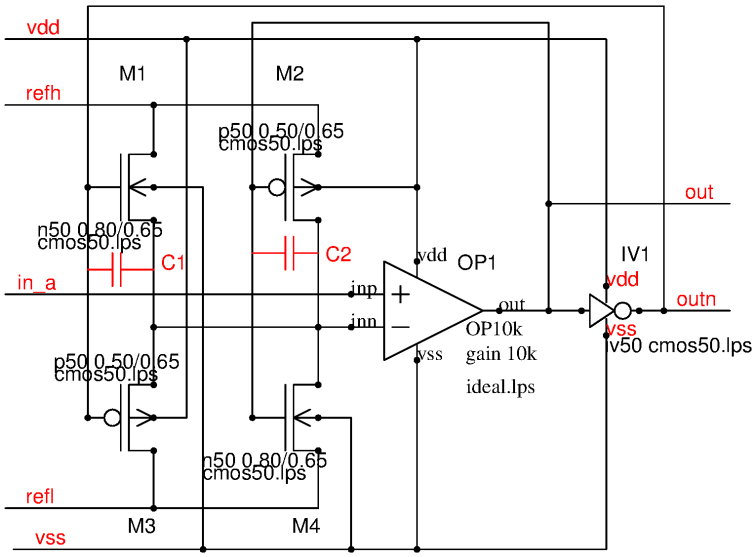

Fig.8: Comparator using one amplifier and transmission gated to produce the hysteresis

In this fairly simple circuit a risk of oscillation is hidden! The miller capacity of the transistors (parasitc capacitors C1 and C2) can act as a feedback that makes the circuit oscillate close to the trip points! To prevent oscillation several measures can be taken:

1. Make the hysteresis as big as possible.
2. Use low resistive sources for refl and refh (RF impedance!).
3. Use minimum transistors for M1 to M4.
4. Match the sizes of the gates (gate capacities) of M1, M4 and M2, M3.
5. A capacity from the negative input of the amplifier to ground reduces feed through of the switching signal into the amplifier.
6. Don't make the amplifier faster than required by the application.
7. Use an amplifier with inherent hysteresis that is bigger than the capacitive feed through spike at the negative input.

8. If nothing helps add a low pass filter between the gates of M1 to M4 and the driving amplifier and inverter.

All these measures must be tested thoroughly simulating the transistor level implementation of the circuit in all corners (fast, slow, hot, cold...)

Comparator with inherent hysteresis provided by the current mirrors: Now we definitely start to build amplifiers that are no more the normal OPAMP style anymore. The following circuit intentionally has a non linear behavior! This is a very efficient solution for building a comparator with hysteresis. Additionally the inherent hysteresis can be used to eliminate capacitive feed through coming from transmission gates. There are many ways to build an inherent hysteresis. The most common way is to add a loop gain higher than 1 to the current mirrors.

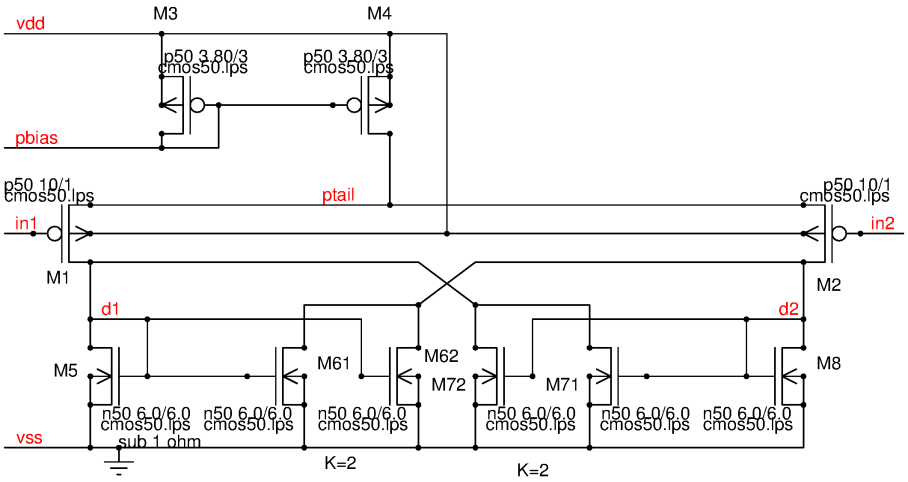

Fig.9 Input stage of a comparator with inherent hysteresis

Exact calculation of the hysteresis is somewhat cumbersome. The equations for the currents of the transistors are:

$$I_{M1} = I_{M5} + I_{M7x} \tag{5}$$

and

$$I_{M2} = I_{M8} + I_{M6x} \tag{6}$$

Plugging in the factor K (ratio of M5 and M6x and M8 and M7x yields:

$$I_{M1} = I_{M5} + K * I_{M8} \tag{7}$$

and

$$I_{M2} = I_{M8} + K * I_{M5} \tag{8}$$

The important question is: What is the condition needed to flip the current mirrors. Let us assume that the current of M2 flows into diode M8. So M7x can sink more K

times more current than M2 provides. M1 only can flip the mirrors when it exceeds the current flowing through M2 by a factor K. The trip points becomes

$$I_{M1trip} = K * I_{M2} \tag{9}$$

The reverse way round works in the same way:

$$I_{M2trip} = K * I_{M1} \tag{10}$$

For M1 and M2 operating in weak inversion the hysteresis of the comparator becomes:

$$V_{hyst} = 2 * \frac{k * T * n}{e} * ln(K) \tag{11}$$

(n is the gate coupling factor as described in chapter 4

$$n = 1 + \frac{C_{bulk}}{C_g} = 1 + \frac{\varepsilon_{si} * t_{ox}}{\varepsilon_{sio_2} * \sqrt{\frac{2 * \varepsilon_{si} * (\phi - V_b)}{q * N_b}}} \tag{12}$$

discussing the MOS transistor equations)

Weak inversion leads to a low hysteresis but this hysteresis unavoidably has a positive temperature coefficient!

To calculate the hysteresis assuming M1 and M2 operate in strong inversion we need to know the bias current (flowing through M4). So at the trip point one transistor operates at

$$I_{M1} = \frac{I_{M4}}{(1 + K)} \tag{13}$$

while the second transistor operates at

$$I_{M2} = \frac{K * I_{M4}}{(1 + K)} \tag{14}$$

$$V_{hyst} = 2 * \Delta V_{gs} = 2 * (\sqrt{\frac{K * I_{M4} * l}{(1 + K) * w * k'}} - \sqrt{\frac{I_{M4} * l}{(1 + K) * w * k'}}) \tag{15}$$

$$V_{hyst} = 2 * (\sqrt{K} - 1) * \sqrt{\frac{I_{M4} * l}{(1 + K) * w * k'}} \tag{16}$$

In this equation l is the length, w the width of the transistors M1 and M2. k' is the transconductance of this specific transistor type.

From the equation we can see that the hysteresis in strong inversion changes with the bias current and k' (which is a function of the gate oxide thickness). Thus the inherent hysteresis provided by a current mirror with positive feedback (K>1) is not a good solution for for high precision applications. To a certain extent the hysteresis can be tweaked to be more constant giving the bias current I_{M4} a negative temperature coefficient (because k' usually decreases with temperature due to the decrease of the mobility of the carriers at increasing temperature).

Note that for very high numbers of K the ratio $\frac{\sqrt{K}-1}{\sqrt{1+K}}$ saturates and the hysteresis can never exceed

$$V_{hystmax} < 2 * \sqrt{\frac{I_{M4} * l}{w * k'}} \tag{17}$$

(This is twice the gate overdrive the transistors of the differential amplifier need to take over the complete bias current.)

So now we arrived at a solution that is cheap, has no static kick back, is independent of supply - but we added a hysteresis again that degrades accuracy. This can be fixed combining the circuit with clocking. But clocked comparators are something I want to address in my next post. Citing one of the Dilbert comics: "I don't want to make your head explode by giving you all the details right now".

References

[1] "Designing Analog Chips", Hans Camenzind, February 2005