Operational Amplifiers part 5: chopper stabilized OPAMP

June 15, 2019

Up to now I have described more or less classical approaches of building an OPAMP. The topologies shown have certain accuracy limits. Offset voltages below 1mV are hard to achieve. Trimming the amplifier is an option, but low cost molded packages with significant mechanical stress limit the benefit of trimming. Devices trimmed correctly on the wafer show significant deviations again after packaging.

1 Chopper stabilized OPAMPs

Chopper amplifiers are in use at least since 1949 [1, 2] . Even chopper amplifiers using magnetic field plates as chopping elements are already described in 1967 [1]! In the beginning chopping was used to eliminate the drift of valve-amplifiers. Transistor amplifiers have a significantly lower drift and statistical offset, but as soon as offsets below 1mV are required either chopping techniques or auto zero techniques become mandatory.

Chopper amplifiers are used for two reasons:

1. Remove amplifier offsets from the signal chain
2. Fold 1/f noise out of the signal bandwidth

The input signal is converted into an AC signal by the input mixer. The amplifier amplifies both, it's own noise and offset as well as the input signal that was folded around the chopper frequency. The second mixer at the chopper amplifier output folds the noise and the offset to around the carrier and it's harmonics and the input signal back from left and right of the chopper frequency to DC and baseband.

Typically a chopper amplifier uses a switch modulator instead of a Gilbert cell. (Theoretically a Gilbert cell can be used as well, but since a Gilbert cell depends on matching it has offset too and there is no more benefit.)

Frequencies close to the chopper frequency can be folded into the use-bandwidth. This is something that is not desired. A chopper amplifier MUST have an analog anti aliasing filter at the input and at the output with a bandwidth significantly less than half of the chopper frequency.

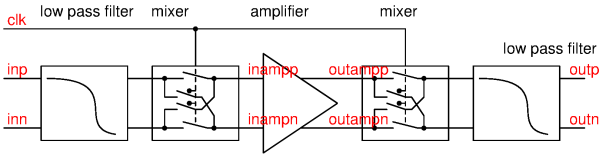

Fig.1: Concept of a chopper amplifier

Besides this fully differential approach single ended (asymmetrical) switching can be found as well. But asymmetric switching only works for fairly low performance requirements. For this reason asymmetrical designs are no more used today. A second reason for no more using asymmetrical modulators is that a perfectly symmetrical modulator also removes the clock. The multiplication of clock and signal without any DC component at the clock input (perfect 50% duty cycle) is a dual side band modulation with suppressed carrier

The following figure shows a simplified spectral representation of the signal.

After the first mixer the signal is folded around the clock. (the clock is a rectangular signal. So we have harmonics at (1+2N)fclk (N=0,1,2,3..) that are neglected in the simplified drawing). The clock frequency itself will only be present when the base band signal holds a DC component.

At the amplifier output before the second mixer we will find the amplified side bands (green), The amplified white noise (red), the 1/f noise of the amplifier (red, dashed fill) and the amplified offset of the amplifier at f=0.

After the second mixer the signal and the white noise are folded back to the base band. (green and red filled). The offset and the 1/f noise are folded to the clock frequency (offset) and into the side bands around the clock frequency.

The low pass filter at the output removes the 1/f noise and the offset that is folded around the clock frequency. Only the amplified signal (with green fill) and the amplified white noise (red fill) are present at V(outp, outn). Since the 1/f noise usually is much bigger than the resistive noise for frequencies below 10kHz this trick to get rid of the 1/f noise is quite versatile.

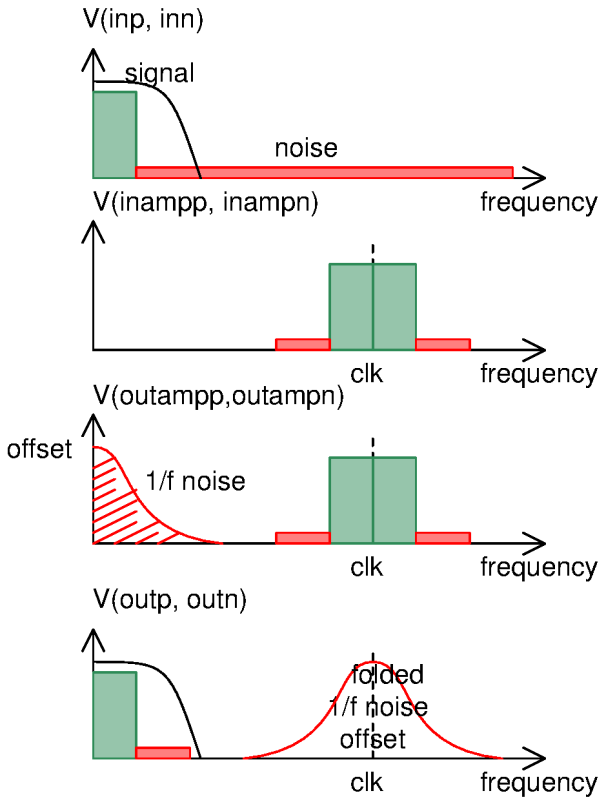

Fig.2: Spectral distribution of the signals at different positions of the signal chain

The advantages of chopping are paid with requirements for the amplifier and the switches:

1. The amplifier bandwidth must be significantly higher than the chopping frequency. (Theoretical minimum 3 times the base band bandwidth, typically 10 times the base band bandwidth!)
2. Due to the high bandwidth the amplifier has a high current consumption.
3. The switches must be designed for low clock feed through.
4. To cancel remaining clock feed through the slew rates of the amplifier for rising and falling edge must match
5. The offset reduction is limited by accuracy of the duty cycle of the clock. It must be as close to 50% as possible

2 Clock generation for a chopper amplifier

The remaining offset error caused by duty cycle deviations is:

$$V_{oschopper} = V_{osop} * D - V_{osop} * (1 - D)$$

$$V_{oschopper} = V_{osop} * (2 * D - 1) \quad (1)$$

Equation 1 shows that D must be 50%. A deviation of only 1% will already reduce the offset reduction to just 1/50 th of the original offset of the amplifier operated without chopping.

Typically the clock signal is generated by a flip flop acting as a divider and a pulse synchronizer eliminating the propagation delay differences between the q and qn output of the flip flop.

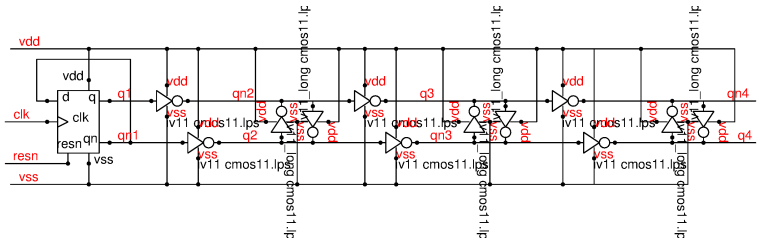

Fig.3: Divider with successing synchronizer latches

The long channel inverters act as a load for the path with the leading edge and as a speed up for the path with the trailing edge.

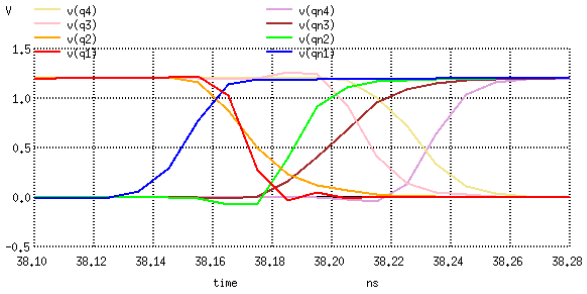

Fig.4: Simulation of the synchronizer chain

The figure above shows how the synchronizer moves the crossing of qx and qnx more and more into the middle with every stage. At the output of the flip flop the crossing was at 1V (falling edge was later than the rising edge.) After the 4th stage the crossing of the opposite signals is already at 0.5V.

2.1 Clock jitter

Clock jitter converts the offset of the amplifier into noise. For this reason the amplifier should already have a low offset even without chopping and the clock should come from a stable source (preferably a quartz oscillator)

3 Summary

Probably the most important argument for building a chopper amplifier instead of an auto zero amplifier is the folding of the 1/f noise out of the baseband. The synchronous demodulator at the output of the amplifier folds the 1/f noise into the side bands of the chopping frequency. The following analog low pass filter finally removes the noise from the signal. The beauty of noise folding has a price. The amplifier must almost perfectly settle during half of a clock period. For precision applications the bandwidth of the amplifier should be:

$$BW_{amp} > 10 * f_{clk}$$

The consequence of the high bandwidth requirement is a high current consumption of the amplifier.

The high clock quality requirements of the chopper amplifier limit the offset reduction. Making the clock slower reduces most of the propagation delay asymmetries of the clock signal but this also reduces the bandwidth of the complete system (remember, $f_{clk} < 2 * BW_{lowpass}$) . Chopping a poor amplifier will only lead to mediocre results. To achieve good results the amplifier as well as the clock generation must already meet high quality standards.

References

[1] "Schaltungen mit Halbleiterbauelementen Band 3", Erich Gelder, Walter Hirschmann, Siemens AG, 1967

[2] "OP AMP Applications", Walter G Jung, Analog Devices Inc. 2002