Operational Amplifiers part 3: rail to rail input

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The lower the supply voltage of an operational amplifier the more attractive it gets to build a rail to rail input stage to maintain a common mode range that is as wide as possible. The rail to rail input basically is a composition of two OTAs (operational transconductance amplifiers) and an addition of the output currents. One of the OTAs has a PMOS input that is ground compatible. The other one of the OTAs has an NMOS input that is supply compatible.

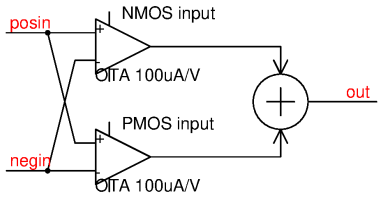

Fig.1: concept of a rail to rail input

Both input stages are folded cascode differential stages to make the common mode range reach the supply rails. The amplifier has 3 operating ranges:

1. Below about 1V only the amplifier with the PMOS input is operating.
2. Between about 1V and vdd-1V both amplifiers are operating and the transconductance of both stages will be added. The total gate area of the differential stage is bigger than in the other operating ranges. Usually the statistical offset is significantly better in this operating range.
3. Above vdd-1V only the amplifier with the NMOS input is working.

Having different gains in the different operating ranges leads to issues regarding the frequency compensation. For this reason usually the bias current of the still operating path is increased below 1V and above vdd-1V to circumvent this unwanted behavior. In addition the aspect ratios of the NMOS transistors and the PMOS transistors of the input stages are adjusted to compensate the different mobility of holes and electrons.

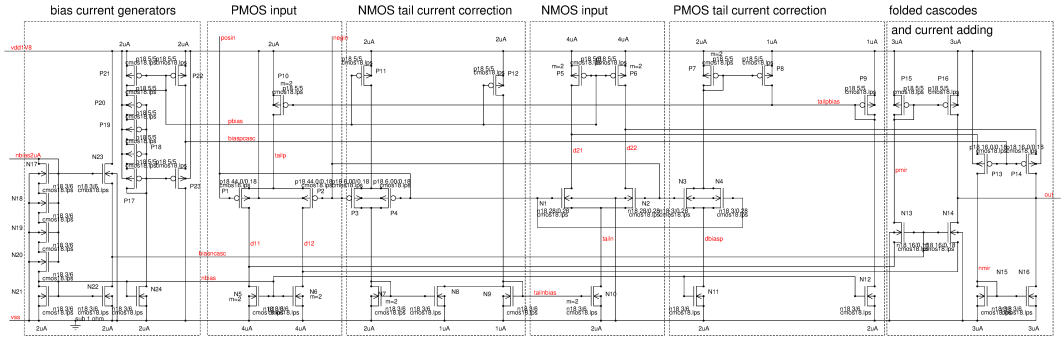

Fig.2: Rail to rail input

The rail to rail input shown above consists of the two differential stages P1, P2 and N1, N3. The transistors P3, P4 and N3, N4 are required to measure the common mode voltage. Current mirrors N7, N8 and P7, P8 reduce the tail currents of the differential stages as long as both differential stages operate within their common mode ranges. If the PMOS input stage leaves its common mode range P3, P3, N7, N8 turn off and the tail current of the NMOS stage increases to compensate the loss of gm. Vice versa if the NMOS input stage leaves the common mode range N3, N4 and P7, P8 turn off and the currents flowing in the PMOS stage increase.

The output currents in this simple example are added at node out. In a full blown amplifier this adding of currents is a bit more complex. In stead of just adding in one node the output currents of the folded cascode stages are used to drive a translinear output stage. This translinear stage has a quadratic characteristic and operates almost in class AB mode. This way a higher gain and higher output drive capability can be achieved. But including the translinear stage in this drawing would have made the whole circuit a bit too complex to serve as a simple example to explain the concept.

The scaling of N5, N6 and P5, P6 is not accidental. The ratio of the currents between the tail and the current mirrors must be bigger than the current increase to keep the folded cascode operating even if the tail currents reach its extremes. This however increases the impact of the current mirror mismatch on the input offset of the amplifier. The input stage operates at $1/4$ of the currents flowing in the folded cascode bias generator! The relative error of the current mirrors will be multiplied by 4 instead of the ideal factor 2 that can be chosen without the tail current correction.

Calculation of statistical errors is still possible similar to the simple folded cascode amplifier. But since now we have two signal paths and a total of 4 current generator pairs, two differential stages and 2 folded cascode pairs involved it makes more sense to use a spread sheet than to write everything into a single equation that requires several lines.

Comparing the most simple amplifiers used in 2.5V to 5V technologies, folded cascodes amplifier used for lower supply voltages and full blown rail to rail amplifiers the efforts are:

type	simple	folded cascode	rail to rail
transistors	8	19	48
relative	1	2.4	6

May be this looks a bit too simple because not all transistors have the same size. But since the error propagation gets worse going to a rail to rail design the cost of a rail to rail topology will in most cases be even more then only 6 times higher than a simple low cost amplifier without rail to rail capability. Adding the effort of the translinear stage the ratio for the rail to rail amplifier approaches values in the range of 8..12 compared to the most simple design possible. Rail to rail amplifiers should only be used where it really is necessary.